CY8CKIT-035

PSoC® 3 and PSoC 5LP Power Supervision Expansion Board Kit (EBK) Guide

Doc. #: 001-86225 Rev. *B

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

Copyrights

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Datasheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable'.

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Contents

1. Introduction

Power supervision plays a critical role in modern communication and industrial systems, such as routers, switches, storage systems, servers, base stations, industrial automation equipment, and medical imaging equipment. Power supervision is a combination of sequencing, monitoring, and controlling of multiple power supply rails that are required for various components in these systems. Power supervision solutions require:

- Rapid fault detection in high-availability systems
- Accurate and reliable power rail sequencing during power-on and power-off events
- Voltage and current measurement to optimize power consumption and for data logging
- Closed-loop control through trimming; margining of voltage rails in the system for development and manufacturing test purposes

The CY8CKIT-035 PSoC® 3 and PSoC 5LP Power Supervision Expansion Board Kit (EBK) together with the example projects demonstrate the system power supervision functions and capabilities of PSoC 3 and PSoC 5LP devices. You can modify the example projects using Cypress's PSoC Creator™ software (included with this kit) and customize them for your own system power supervision needs.

The Power Supervision EBK is designed to work with any of the three PSoC Development Kits (DVKs) - PSoC 3 Kit (CY8CKIT-030), PSoC 5LP Kit (CY8CKIT-050), or PSoC Kit (CY8CKIT-001). This document describes the use of the example projects on each of these kits.

For information on the PSoC 1 power supervision solution using this kit, refer to the PSoC 1 Power Supervision Kit Guide located at www.cypress.com/go/CY8CKIT-015.

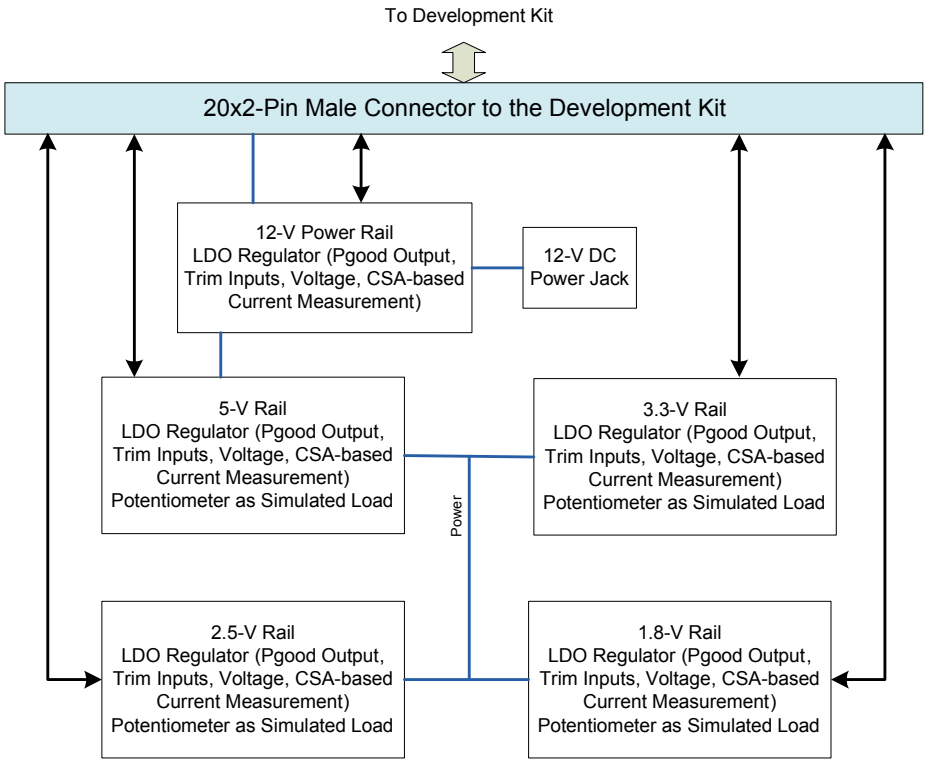
1.1 Features

The CY8CKIT-035 Power Supervision EBK provides a platform to develop power management and supervision solutions with PSoC 3 and PSoC 5LP devices that include the following features:

- Power supply sequencing
- Power supply voltage and current measurement
- Power supply voltage trimming and margining
- Power supply over-voltage and under-voltage fault detection
- I2C, SMBus, and PMBus host communications interface

Figure 1-1 shows a simplified block diagram of the fundamental components of the Power Supervision EBK. Not all hardware components are shown.

Figure 1-1. Power Supervision EBK Block Diagram



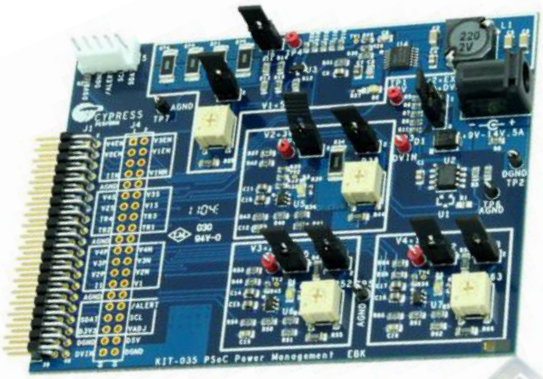
1.2 Kit Contents

The Power Supervision EBK consists of:

- Power Supervision expansion board
- Quick start guide
- Power DC adapter (12 V/2 A)
- PSoC 3 and PSoC 5LP Power Supervision EBK Guide (this document)
- PSoC Creator and prerequisite software
- PSoC Programmer™ and prerequisite software
- PSoC Power Supervision Tool
- Example projects for the PSoC Kit (CY8CKIT-001)
  - Advanced sequencer
  - Power supervision
- Example projects for the PSoC 3 Kit (CY8CKIT-030)
  - Advanced sequencer
  - Power supervision
- Example projects for the PSoC 5LP Kit (CY8CKIT-050)
  - Advanced sequencer
  - Power supervision

Note This kit can also be used to evaluate PSoC 1-based power supervision solution. See the PSoC 1 Power Supervision EBK Guide located at www.cypress.com/go/CY8CKIT-015 for more details.

Figure 1-2. Power Supervision EBK Package Contents



Power Supervision Evaluation Board

Quick Start Guide

DC Power Adapter 12 V/2 A

1.3 PSoC Creator

Cypress's PSoC Creator software is an easy-to-use integrated development environment (IDE) that introduces a hardware and software design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Draw a schematic of the hardware circuit you want to build inside PSoC; the tool will automatically place and route the components.
- Eliminate external CPLDs or standard logic ICs by integrating state machines and simple glue logic in your design.
- Trade-off architecture decisions between hardware and software, allowing you to focus on what matters in getting you to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support PSoC 3 and PSoC 5LP.

1.4 Additional Learning Resources

For more details on the kit, visit http://www.cypress.com/go/CY8CKIT-035.

For support, visit http://www.cypress.com/go/support or contact us on +1-800-541-4736 Ext. 2 (USA) or +1-408-943-2600 Ext. 2 (International).

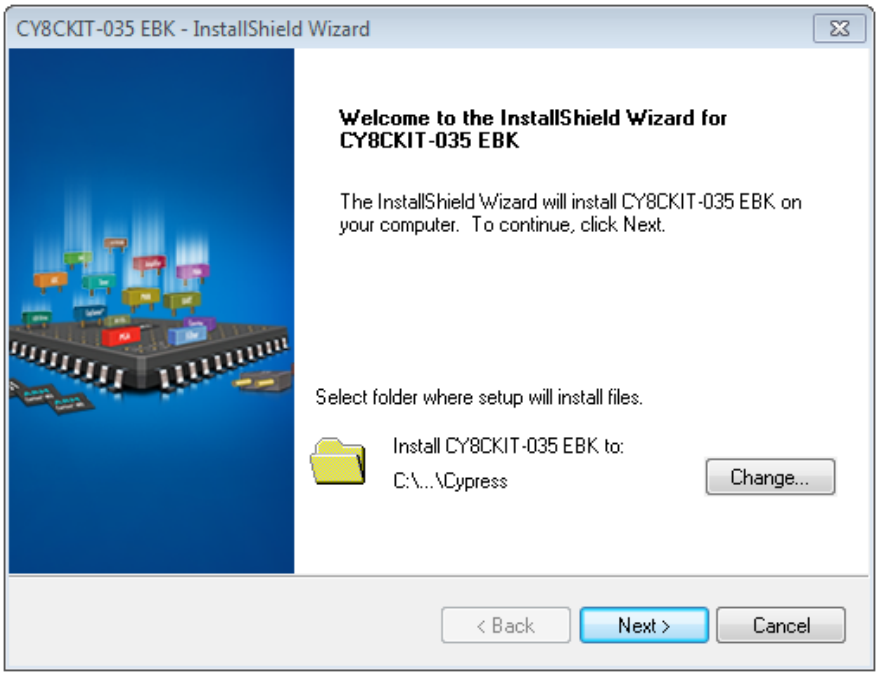
2. Software Installation

2.1 Install Kit Software

Follow these steps to install the PSoC Power Supervision EBK software:

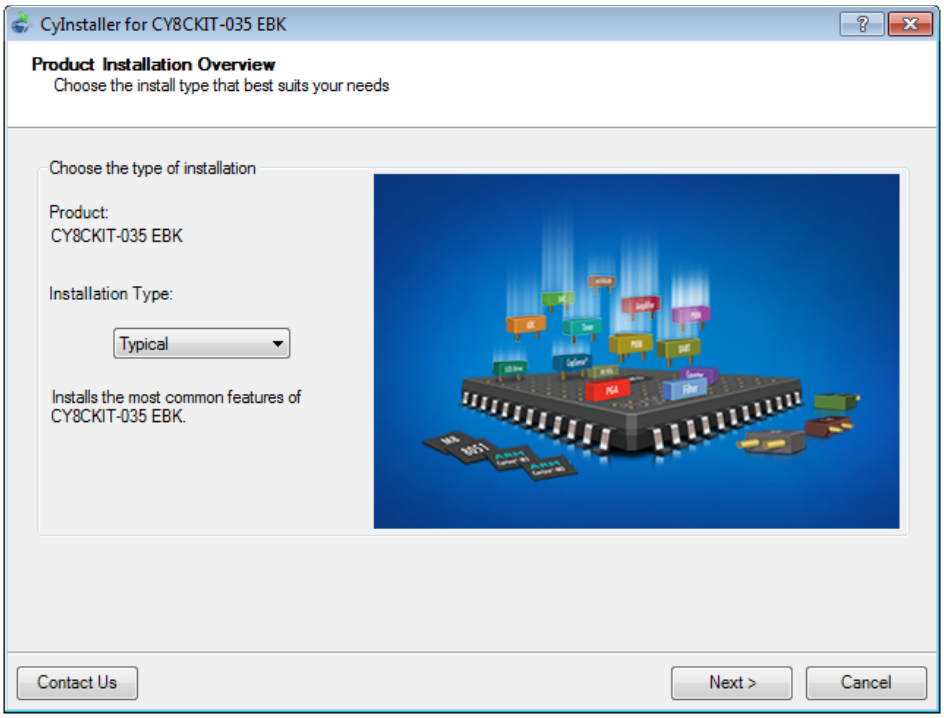
1. Download and install the PSoC Power Supervision EBK software from www.cypress.com/go/CY8CKIT-035.
2. Select the folder to install the CY8CKIT-035 related files. Choose the directory and click **Next**.

Figure 2-1. Installation Folder



3. Select the installation type and click **Next**.

Figure 2-2. Installation Type Options



After the installation is complete, the kit contents are available at following location:

`<Install_Directory>\CY8CKIT-035 EBK\<version>`

Note: For Windows 7 users, the installed files and the folder are read-only. To change the property, right-click the folder and select **Properties** > **Attributes**; disable the **Read-only** radio button. Click **Apply** and **OK** to close the window.

2.2 Install Software

Before installing the PSoC Power Supervision EBK, uninstall any existing version first. When installing the PSoC Power Supervision EBK, the installer checks if the required software is installed in the system. If the required applications are not installed, then the installer prompts you to download and install them.

The following software is required:

- PSoC Creator 3.3 Component Pack 1 or later: Download the latest software from www.cypress.com/go/Creator.
- PSoC Programmer 3.23.1 or later: Download the latest software from www.cypress.com/go/Programmer.
- PSoC Power Supervision Tool 2.2 or later: Download the latest software from www.cypress.com/go/CY8CKIT-035.
- Code examples: After the kit installation is complete, the code examples are available in the kit firmware folder. Download the CD ISO image or setup files from www.cypress.com/go/CY8CKIT-035.

After installation is complete, the following are installed on your computer:

- PSoC Creator

- PSoC Programmer
- PSoC Power Supervision Tool
- PMBus User Guide
- Kit documents
  - Quick Start Guide
  - User Guide
- Firmware
  - Example projects for PSoC Creator
- Hardware
  - Schematic
  - Layout
  - Bill of materials (BOM)

2.3 Uninstall Kit Software

The software can be uninstalled using one of the following methods:

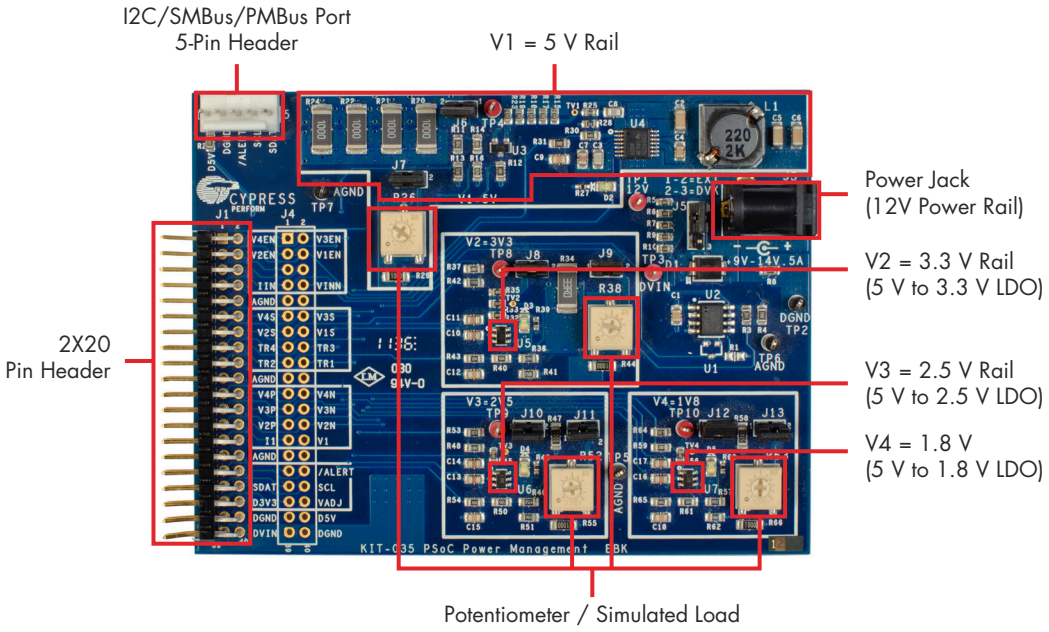
- Go to **Start** > **Control Panel** > **Add or Remove Programs**; select the appropriate software package and click the Remove button.
- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**; select the **Uninstall** button for the appropriate software package.

3. Kit Operation

3.1 Kit Overview

Figure 3-1 shows the CY8CKIT-035 Power Supervision Expansion Board. The board consists of a 12-V primary input power source and four secondary voltage rails. Each secondary rail consists of a regulator with enable input, circuitry that enables PSoC to apply a DC control voltage to the regulator feedback or adjust pin, as well as fixed and adjustable (potentiometer) load elements. Two jumpers are provided for each rail to either disconnect all loads or disconnect only the adjustable load.

Figure 3-1. Power Supervision Expansion Board



Note Voltage rail V1 provides power to the other three rails V2, V3, and V4. Therefore, disabling V1 will disable V2–V4.

The Power Supervision Expansion Board also provides an I2C/SMBus/PMBus connector. A 40-pin (2×20) header J1 is provided to connect this board with the host PSoC on a development kit platform such as the PSoC Kit (CY8CKIT-001), PSoC 3 Kit (CY8CKIT-030), or PSoC 5LP Kit (CY8CKIT-050). The header carries voltage enables, regulator voltage, regulator load currents, and trim/margin control signals for each regulator on the Power Supervision Expansion Board. The I2C physical layer signals (SDA/SCL) from PSoC are also routed across this header to enable connection to an external host or management processor that supports standard I2C, SMBus, or PMBus protocol interfaces. The Power Supervision EBK includes the Power Supervision Tool to work as the external host.

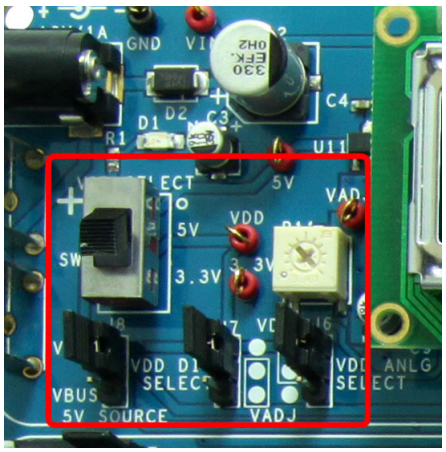
3.2 Kit Connections

This section provides instructions to set up PSoC kits (CY8CKIT-001, CY8CKIT-030, or CY8CKIT-050) for use with the Power Supervision EBK to evaluate the PSoC 3 and PSoC 5LP power supervision solution.

3.2.1 PSoC Kit (CY8CKIT-001)

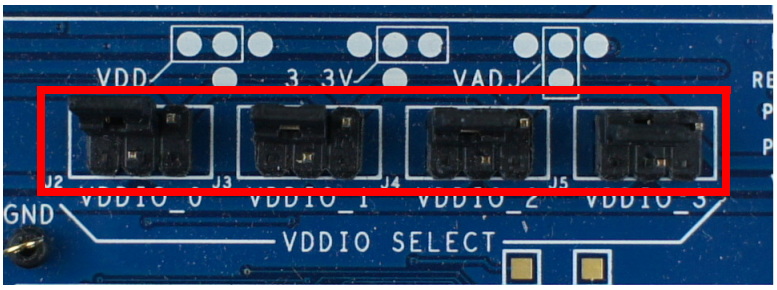
1. Set the system to run at 5 V using SW3; set J6 VDD ANLG and J7 VDD DIG to VDD = 5 V using J6 and J7, as shown in Figure 3-2.

Figure 3-2. PSoC Kit (CY8CKIT-001) Power Jumpers



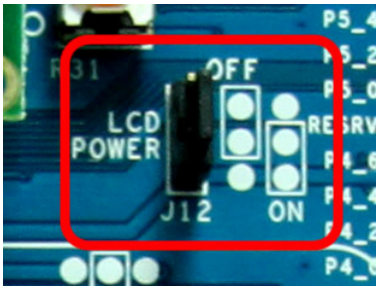
2. Set J2, J3, J4, and J5 to use VDD, as shown in Figure 3-3.

Figure 3-3. J2, J3, J4, and J5 Selected to VDD



3. Ensure that the LCD included with the PSoC Kit is attached and that the LCD power jumper (J12) is in the ON position. All other jumpers should have the default settings.

Figure 3-4. PSoC Kit (CY8CKIT-001) LCD Power Jumper

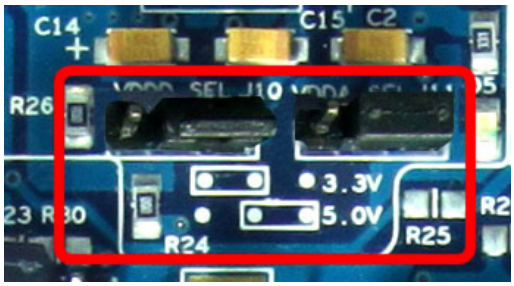


CAUTION Do not attach the Power Supervision EBK to the PSoC Kit until you have programmed the PSoC with one of the example projects. The GPIOs routed to the Power Supervision EBK connect to the power regulator circuits, which may be damaged if firmware previously programmed into PSoC drives those pins. When PSoC has been programmed with the example project (as described in Example Projects on page 27), attach the Power Supervision EBK to port A of the PSoC Kit.

3.2.2 PSoC 3 (CY8CKIT-030) Kit

1. Set VDDD and VDDA to 5.0 V using J10 and J11.

Figure 3-5. PSoC 3 Kit (CY8CKIT-030) Power Jumpers



CAUTION Do not attach the Power Supervision EBK to the PSoC 3 Kit until you have programmed the PSoC with one of the example projects. The GPIOs routed to the Power Supervision EBK connect to the power regulator circuits, which may be damaged if firmware previously programmed into PSoC drives those pins. When PSoC has been programmed with the example project (as described in Example Projects on page 27), attach the Power Supervision EBK to port E of the PSoC 3 Kit.

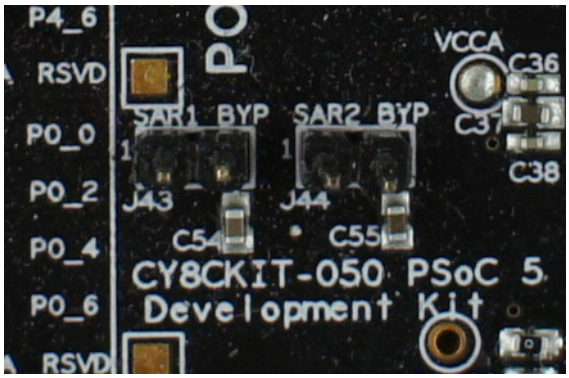
3.2.3 PSoC 5LP (CY8CKIT-050) Kit

1. Set VDD and VDDA to 5.0 V using J10 and J11. All other jumpers should have the default settings.

Figure 3-6. PSoC 5LP Kit (CY8CKIT-50) Power Jumpers

2. Disconnect the SAR bypass jumpers J43 and J44. All other jumpers should have the default settings.

Figure 3-7. PSoC 5LP Kit (CY8CKIT-50) SAR Bypass Jumpers



CAUTION: Do not attach the Power Supervision EBK to the PSoC 5LP Kit until you have programmed the PSoC with one of the example projects. The GPIOs routed to the Power Supervision EBK connect to the power regulator circuits, which may be damaged if firmware previously programmed into PSoC drives those pins. When PSoC has been programmed with the example project (as described in Example Projects on page 27), attach the Power Supervision EBK to port E of the PSoC 5LP Kit.

3.3 Example Projects

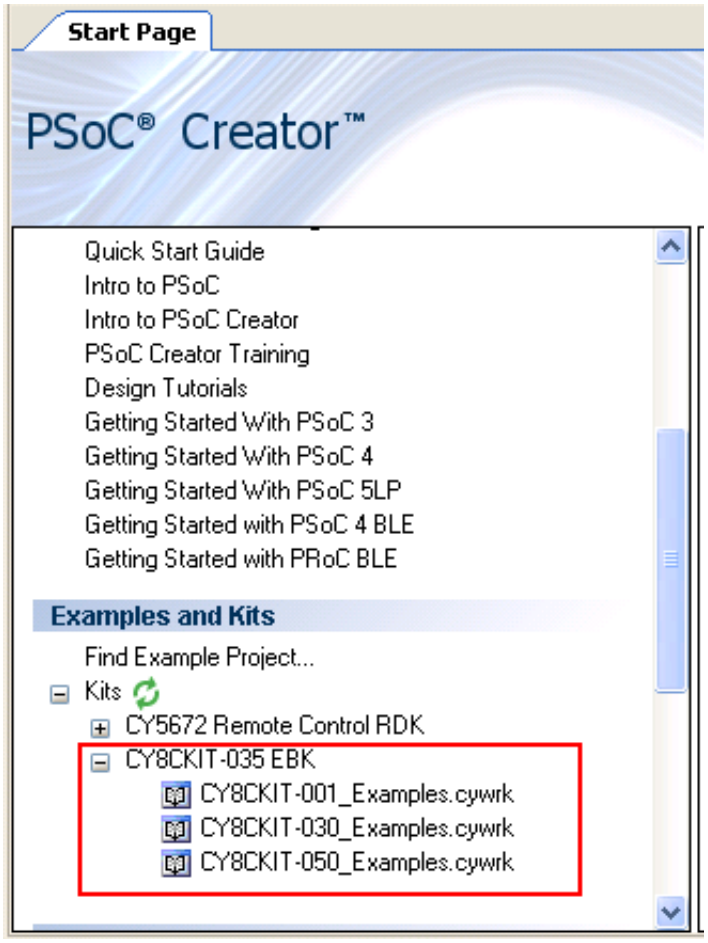
The Power Supervision EBK includes two example projects, which demonstrate the PSoC 3 and PSoC 5LP solution for power supervision:

- Advanced Sequencer: This example demonstrates voltage sequencing and under-voltage (UV) and over-voltage (OV) monitoring using the window comparator for rapid fault detection.
- Power Supervision: This example demonstrates a more comprehensive power supervision solution with power supply trimming, voltage, and current measurements, which are capable of being monitored and controlled over the PMBus interface.

The kit software installs these example projects in PSoC Creator, from where they can be accessed as described here:

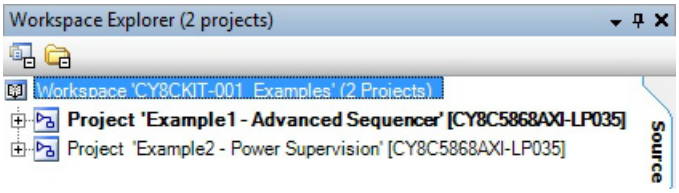
1. Go to **Start Page** in PSoC Creator.
2. In the **Examples and Tutorials** section, expand the **Kits and Solutions** entry, as shown in Figure 3-8.
3. Expand the PSoC Power Supervision EBK entry. There are three project workspaces listed under the entry, as shown in Figure 3-8.
   a. **CY8CKIT-001_Examples.cywrk** workspace contains the two example projects designed to work out of the box with PSoC Kit (CY8CKIT-001).
   b. **CY8CKIT-030_Examples.cywrk** workspace contains the two example projects designed to work out of the box with PSoC 3 Kit (CY8CKIT-030).
   c. **CY8CKIT-050_Examples.cywrk** workspace contains the two example projects designed to work out of the box with PSoC 5LP Kit (CY8CKIT-050).
4. The example projects can be copied to any location you specify on your hard drive and then opened automatically.

Figure 3-8. PSoC Creator Start Page showing Kits and Solutions



5. The example projects are displayed in the **Workspace Explorer** window; Figure 3-9 shows the window for the **CY8CKIT-001_Examples** workspace. To use one of the example projects, right-click on it and select **Set As Active Project**. This will make the selected project as the active one, which can then be programmed into the kit.

Figure 3-9. Workspace Explorer View



3.3.1 Set Up the Example Projects on PSoC Kit (CY8CKIT-001)

Set up the PSoC Kit according to PSoC Kit (CY8CKIT-001) on page 12.

1. If this is the first time that the example project firmware is being programmed into PSoC, make sure that the Power Supervision EBK is not connected to the PSoC Kit.
2. Apply 12-V DC power to the PSoC Kit.

3. To use the example projects with PSoC 5LP, connect the PSoC 5LP Processor Module (CY8CKIT-010) to the PSoC Kit. Connect the MiniProg3 first to a USB port on the PC and then to the PROG port on the PSoC 5LP Processor Module.

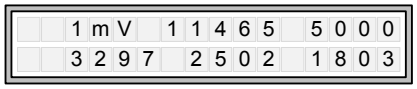
   To use the example projects with PSoC 3, connect the PSoC 3 Processor Module (CY8CKIT-009) to the PSoC Kit. Connect the MiniProg3 first to a USB port on the PC and then to the PROG port on the PSoC 3 Processor Module.
4. In PSoC Creator, select the desired example project from the **CY8CKIT-001_Examples** workspace and set it as the active project. See Figure 3-9.
5. In PSoC Creator, select **Debug > Program** to program PSoC 5LP.[1]

   To use the example project with PSoC 3, right-click on the example project in the Workspace Explorer and select **Device Selector**… In the Devices tab, search for **CY8C3866AXI-040** and click the **OK** button. Then select **Debug > Program** to program the PSoC 3. This will automatically recompile and rebuild the example project to work with PSoC 3.
6. Remove power from the PSoC Kit and attach the Power Supervision EBK to port A of the PSoC Kit.
7. On the Power Supervision EBK, make sure the power jumper (J5) is set to **DVK** (position 2-3, default setting). Populate jumpers J6, J7, J8, J9, J10, J11, J12, and J13.
8. Apply 12-V DC power to the PSoC Kit via J3.
9. With the Example Project 1 (Advanced Sequencer) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the following.

Figure 3-10. Example 1 - LCD Display for Normal Operation

   The four digits indicate the rail failure status (UV or OV). A dash '–' indicates that the rail is within the defined operating limits. If there is a failure on any rail, the corresponding rail number will be displayed next to the UV or OV indicator.
10. With the Example Project 2 (Power Supervision) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the voltage measurements in millivolts.

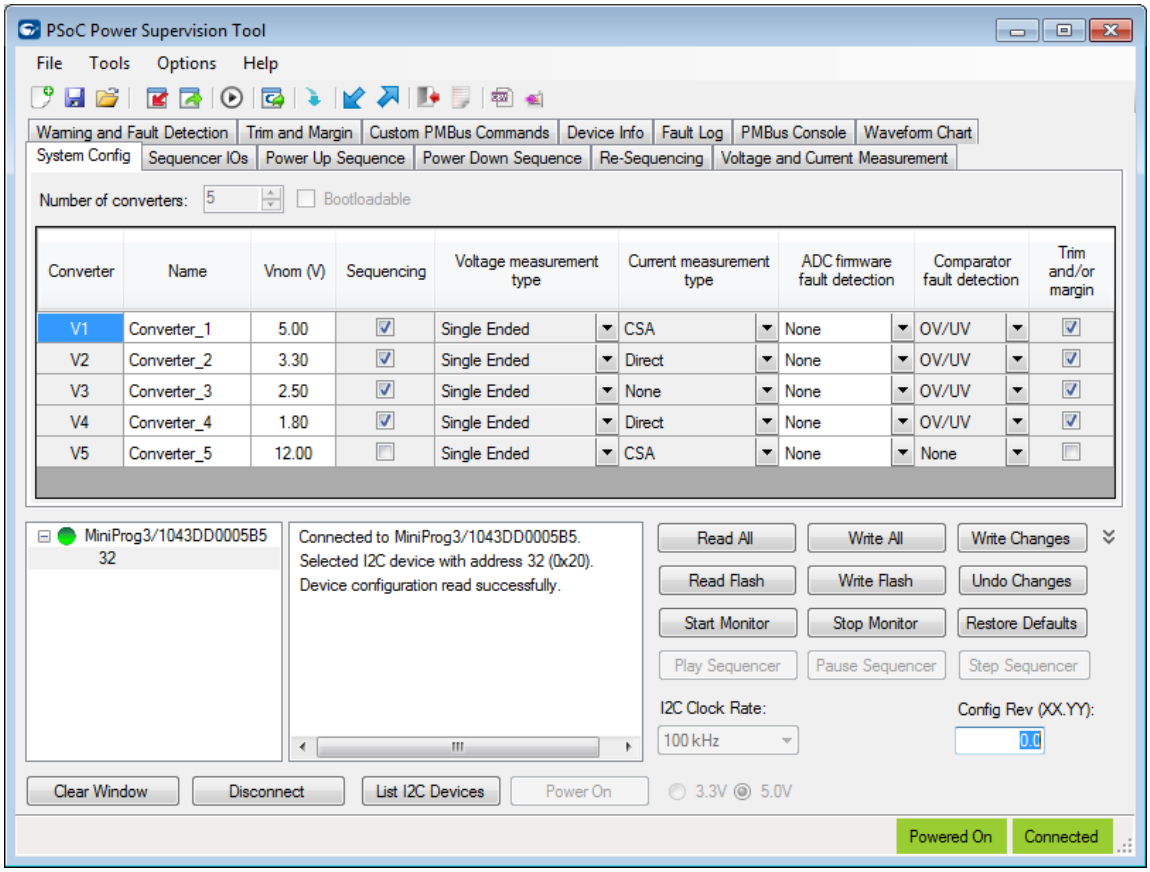
Figure 3-11. Example 2 - LCD Display with Voltage Measurements



11. Connect the MiniProg3 to the white connector (J2) of CY8CKIT-035 and launch the PSoC Power Supervision Tool (**Start** > **All Programs** > **Cypress** > **PSoC Power Supervision Tool**). The tool should automatically connect to the MiniProg3; click the **Read All** button.

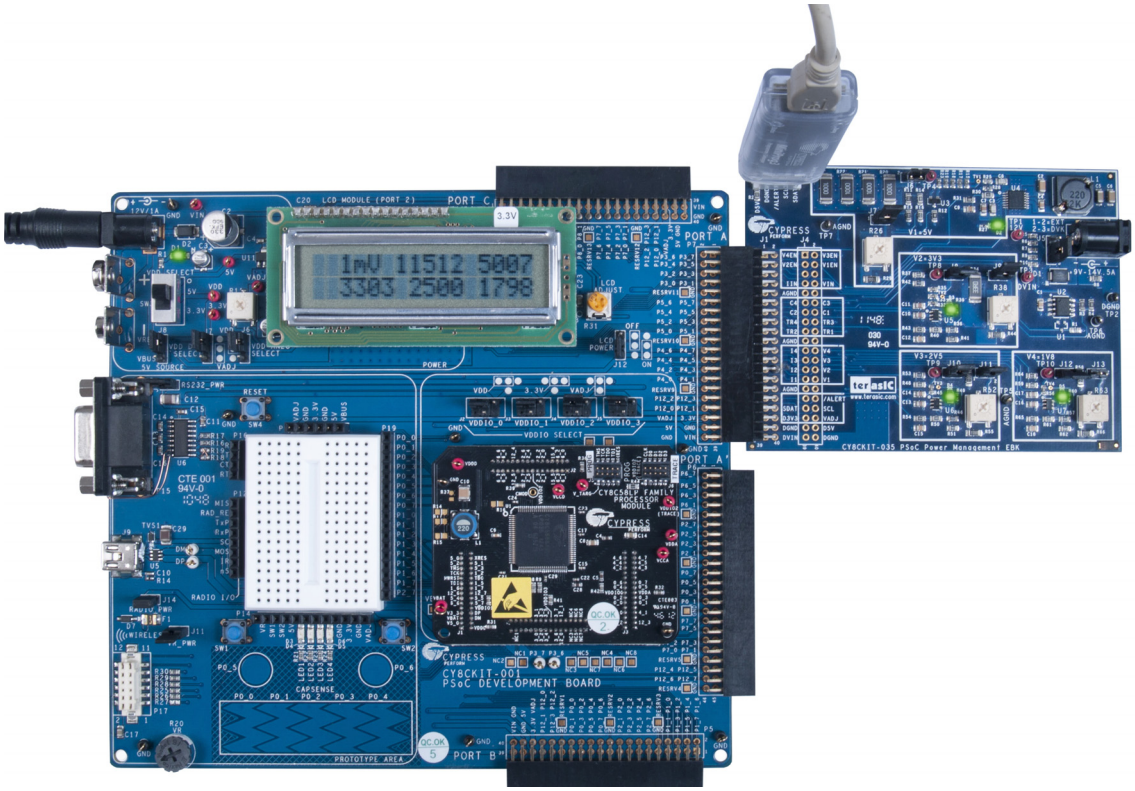
1. PSoC Creator will generate a few notes during the project build. These notes will not affect the functionality of the project. The notes are generated due to the Voltage Fault Detector analog routing constraints.

Figure 3-12. PSoC Power Supervision Tool



For more information on the example projects, see Example Projects on page 27.

Figure 3-13. PSoC Kit (CY8CKIT-001) with Power Supervision EBK Connected to Port A



3.3.2 Set Up the Example Projects on PSoC 3 Kit (CY8CKIT-030)

Set up the PSoC 3 Kit according to instructions in PSoC 3 (CY8CKIT-030) Kit on page 13.

1. If this is the first time that the example project firmware is being programmed into PSoC, make sure the Power Supervision EBK is not connected to the PSoC 3 Kit.
2. Attach a USB cable from the PC to the PSoC 3 Kit Program/Debug USB port (use J1 - the USB connector closest to the corner of the board).
3. In PSoC Creator, select the desired example project from the **CY8CKIT-030_Examples** workspace and set it as active by right-clicking on it in the Workspace Explorer and selecting **Set As Active Project**.
4. In PSoC Creator, select **Debug > Program** to program PSoC.[2]
5. Remove the USB cable from the PSoC 3 Kit and attach the Power Supervision EBK to port E of the PSoC 3 Kit.
6. On the Power Supervision EBK, make sure the power jumper (J5) is set to **EXT** (position 1–2). Note that this is not the default setting for the J5 jumper. Populate all other jumpers (J6, J7, J8, J9, J10, J11, J12, and J13).
7. Apply 12-V DC power to the Power Supervision EBK.
8. With the Example Project 1 (Advanced Sequencer) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the following.

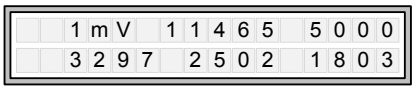
2. PSoC Creator will generate a few notes during the project build. These notes will not affect the functionality of the project. The notes are generated due to the Voltage Fault Detector analog routing constraints.

Figure 3-14. Example 1 - LCD Display for Normal Operation

The four digits indicate the rail failure status (UV or OV). A dash '-' indicates that the rail is within the defined operating limits. If there is a failure on any rail, the corresponding rail number will be displayed next to the UV or OV indicator.

9. With the Example Project 2 (Power Supervision) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the voltage measurements in millivolts.

Figure 3-15. Example 2 - LCD Display with Voltage Measurements



10. Connect the MiniProg3 to the white connector (J2) of CY8CKIT-035 and launch the PSoC Power Supervision Tool (**Start** > **All Programs** > **Cypress** > **PSoC Power Supervision Tool**). The tool should automatically connect to the MiniProg3; click the **Read All** button.

Figure 3-16. PSoC Power Supervision Tool

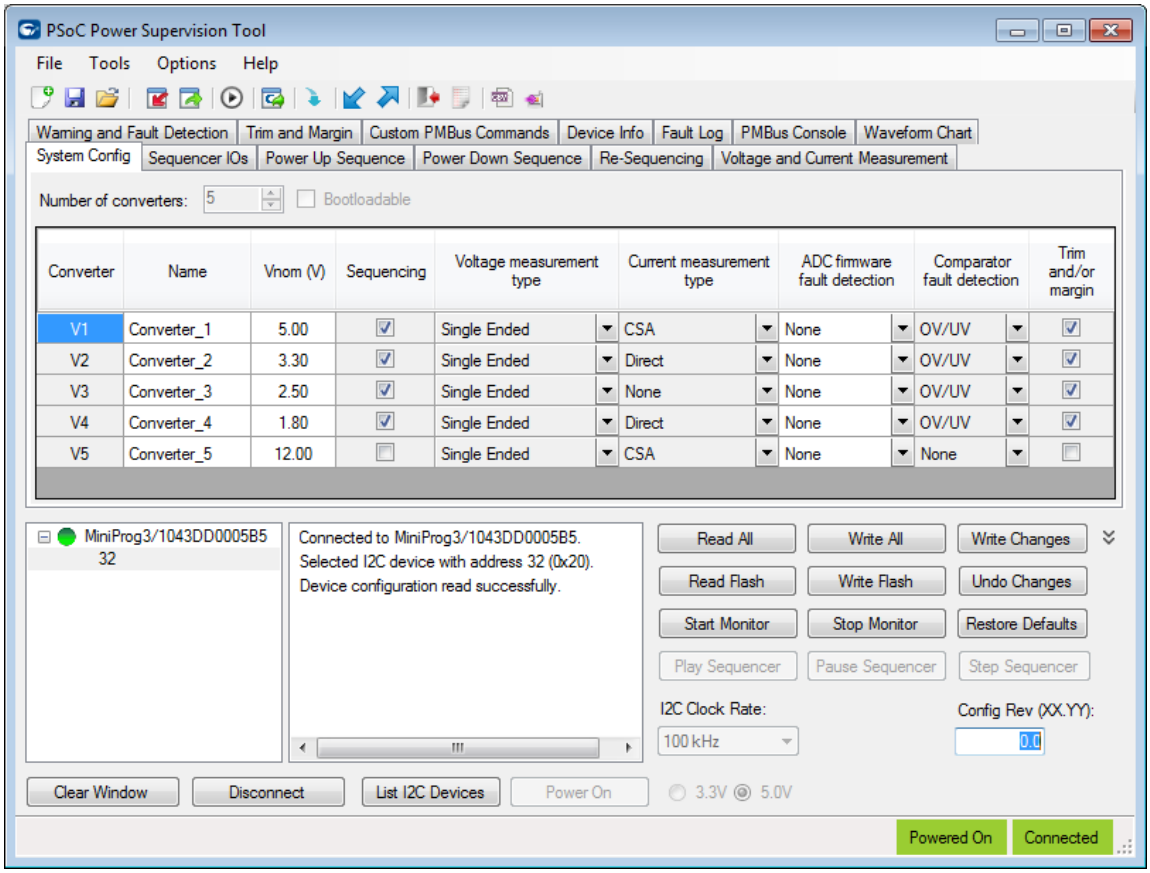
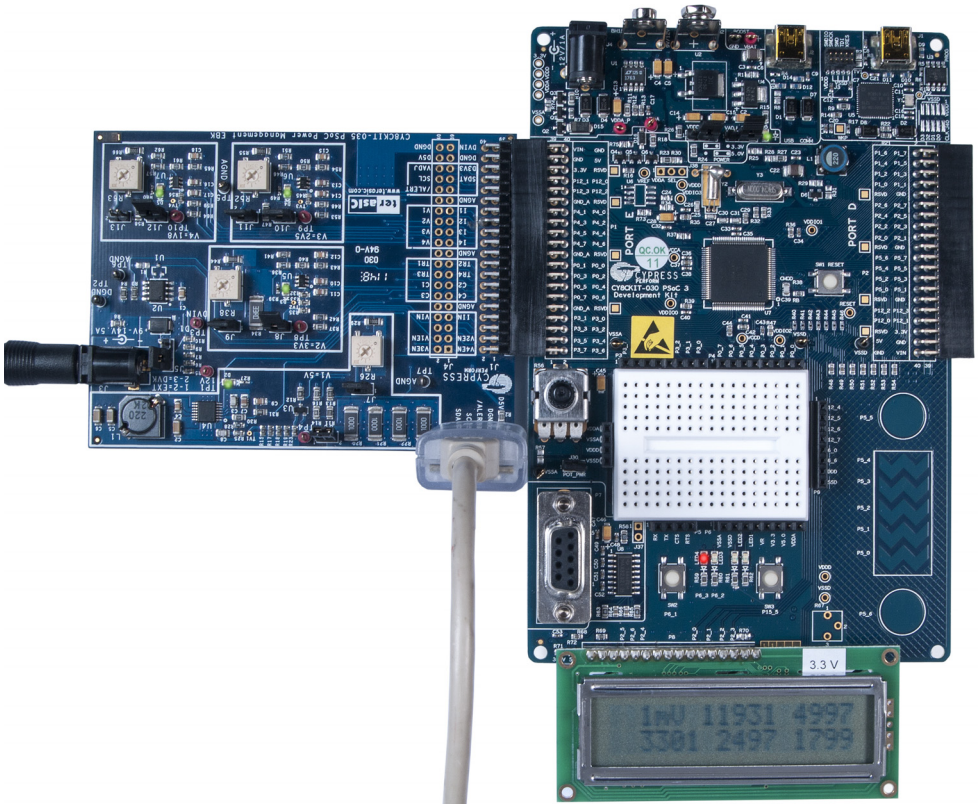


Figure 3-17. PSoC 3 Kit (CY8CKIT-030) with Power Supervision EBK Connected to Port E



3.3.3 Set Up the Example Projects on PSoC 5LP Kit (CY8CKIT-050)

Set up the PSoC 5LP Kit according to instructions in PSoC 5LP (CY8CKIT-050) Kit on page 13.

1. If this is the first time that the example project firmware is being programmed into PSoC, make sure the Power Supervision EBK is not connected to the PSoC 5LP Kit.
2. Attach a USB cable from the PC to PSoC 5LP Kit Program/Debug USB port (use J1 - the USB connector closest to the corner of the board).
3. In PSoC Creator, select the desired example project from the **CY8CKIT-050_Examples** workspace. Set the example project as active by right-clicking on it in the **Workspace Explorer** and selecting **Set as Active Project**.
4. In PSoC Creator, select **Debug > Program** to program PSoC.[3]
5. Remove the USB cable from the PSoC 5LP Kit and attach the Power Supervision EBK to port E of the PSoC 5LP Kit.
6. On the Power Supervision EBK board, make sure the power jumper (J5) is set to **EXT** (position 1-2). Note that this is not the default setting for the J5 jumper. Populate all other jumpers (J6, J7, J8, J9, J10, J11, J12, and J13).
7. Apply 12-V DC power to the Power Supervision EBK.
8. With the Example Project 1 (Advanced Sequencer) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the following.

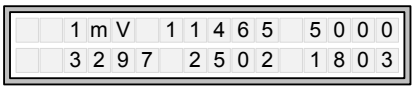
3. PSoC Creator will generate a few notes during the project build. These notes will not affect the functionality of the project. The notes are generated due to the Voltage Fault Detector analog routing constraints.

Figure 3-18. Example 1 - LCD Display for Normal Operation

The four digits indicate the rail failure status (UV or OV). A dash '-' indicates that the rail is within the defined operating limits. If there is a failure on any rail, the corresponding rail number will be displayed next to the UV or OV indicator.

9. With the Example Project 2 (Power Supervision) set up properly, all four green LEDs on the Power Supervision EBK should be turned on and the LCD should show the voltage measurements in millivolts.

Figure 3-19. Example 2 - LCD Display with Voltage Measurements



10. Connect the MiniProg3 to the white connector (J2) of CY8CKIT-035 and launch the PSoC Power Supervision Tool (**Start** > **All Programs** > **Cypress** > **PSoC Power Supervision Tool**). The tool should automatically connect to the MiniProg3; click the **Read All** button.

Figure 3-20. PSoC Power Supervision Tool

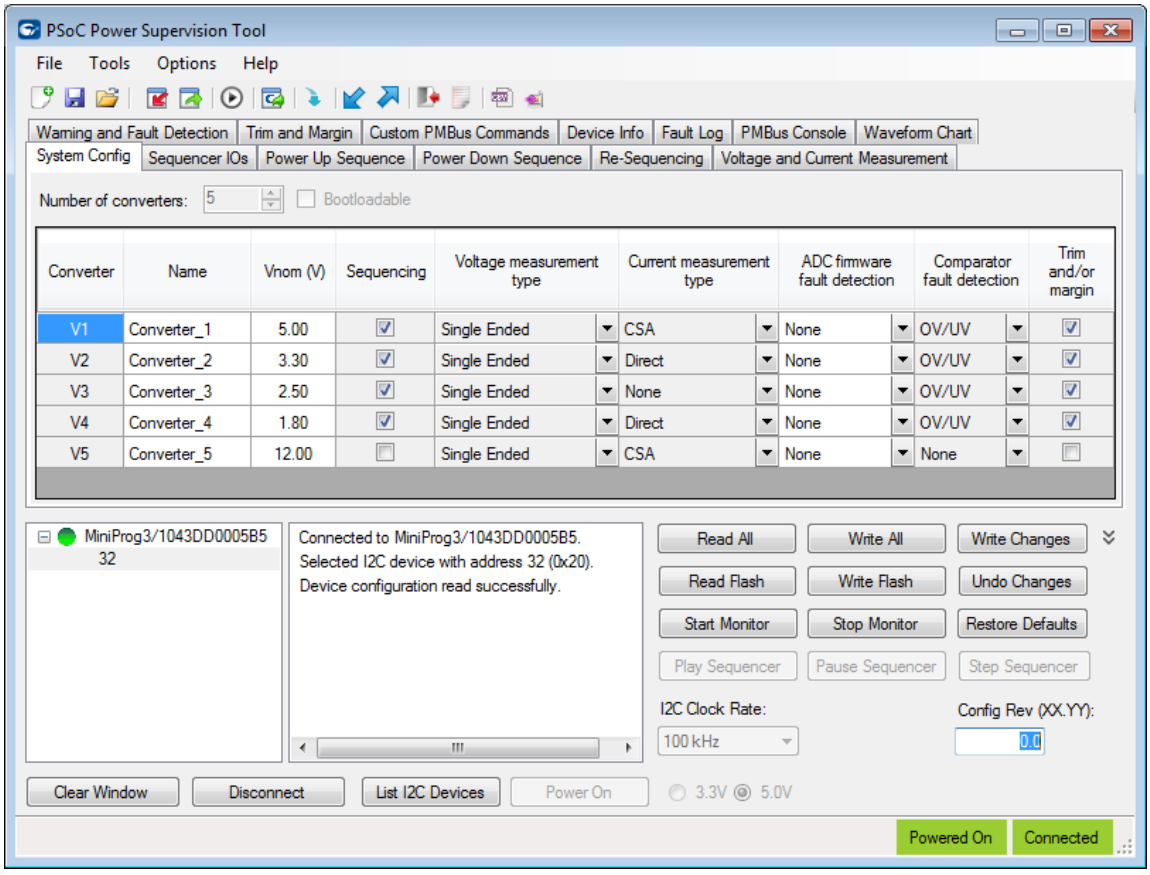
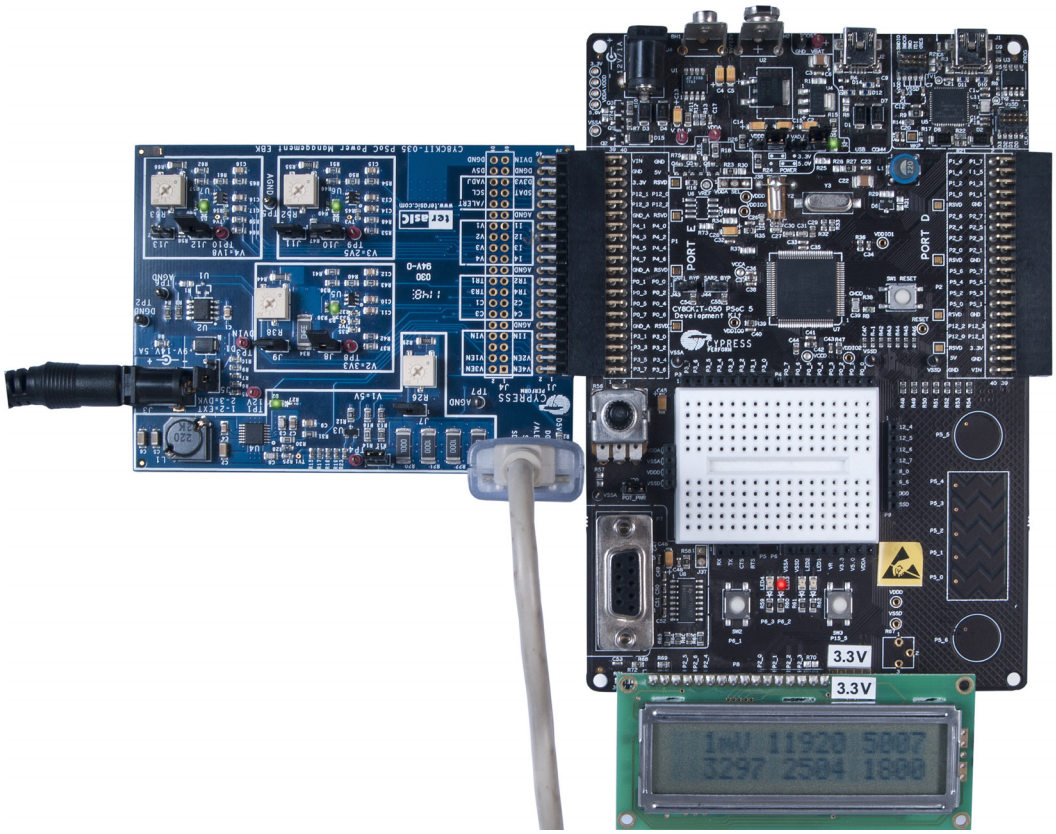


Figure 3-21. PSoC 5LP Kit (CY8CKIT-050) with Power Supervision EBK Connected to Port E



4. Kit Hardware

4.1 PSoC 4+1 Power Supervision Solution

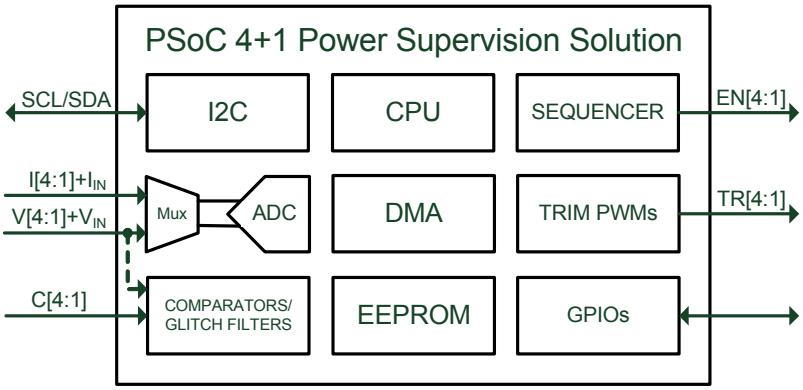
The Power Supervision EBK contains four DC voltage regulator circuits. This kit allows PSoC to control the power-up and power-down sequencing of the regulators. The regulators also have the passive components to enable PSoC to measure their output voltage and load currents using its built-in analog-to-digital converter (ADC). The output voltage of the regulators are trimmed (or margined) by PSoC. PSoC can detect under-voltage and over-voltage fault conditions using its internal window comparator hardware. The Power Supervision EBK also provides an I2C/SMBus/PMBus compatible header to support systems that require communication with a host controller. All of this is implemented on a single PSoC 3/PSoC 5LP.

The Power Supervision EBK routes the input and output signals for power management or power supervision to a PSoC 3 or PSoC 5LP mounted on a development kit platform such as the CY8CKIT-001 PSoC Kit, CY8CKIT-030 PSoC 3 Kit, or CY8CKIT-050 PSoC 5LP Kit. PSoC 3 or PSoC 5LP is not mounted on the Power Supervision EBK.

Figure 4-1 shows a high-level overview of the 4+1 power supervision solution that can be implemented using the Power Supervision EBK. Up to four secondary regulators can be sequenced through the logic-level enable outputs (labeled as EN[4:1]). The four secondary voltage rails along with one primary input power rail (labeled as V[4:1]+V_{IN}) can be multiplexed into a 12-bit, differential delta-sigma ADC configured for a single-ended input range of 0 to 4096 mV at 27 ksps with a 0.1 percent accurate internal reference. For load current measurements across a series shunt resistor (labeled as I[4:1]+I_{IN}), the ADC configuration is dynamically changed to a differential input range of ±128 mV at 22.9 ksps (samples per second). A firmware interrupt service routine (ISR) running on PSoC is responsible for taking the raw ADC readings and converting them to actual voltages (in mV) and currents (in µA), performing simple IIR filtering and using this information to increase or decrease the duty cycles of the pulse-width-modulated (PWM) outputs for regulator trimming and margining. The trim/margin PWM outputs from PSoC (labeled as TR[4:1]) are filtered with a single RC filter stage on the Power Supervision EBK and fed into the voltage feedback input of the regulators.

A single time-multiplexed window comparator is implemented in PSoC using two voltage digital-to-analog converters (DAC) (to set the under- and over-voltage limits for each rail), two comparators, and a programmable glitch filter. This window comparator loops through each channel at 4 µs per channel. Note that there are four dedicated comparator inputs (labeled C[4:1]), which can be multiplexed into a window comparator. It is also possible to use the V[4:1] inputs instead of the C[4:1] inputs to connect to the window comparator.

Figure 4-1. 4+1 Power Management Functional Diagram



Note that the Power Supervision EBK hardware limits support up to a maximum of four secondary regulator circuits. The PSoC 3 or PSoC 5LP power supervision solution can be easily extended to support up to 16 secondary regulator circuits. Contact Cypress for further information on the full 17-rail power supervision solution.

4.2 Layout and Components

Figure 4-2 and Figure 4-3 show pictures of the Power Supervision EBK, depicting the board layout and indicating locations of the connectors and other key components.

Figure 4-2. Power Supervision EBK PCB (Top)

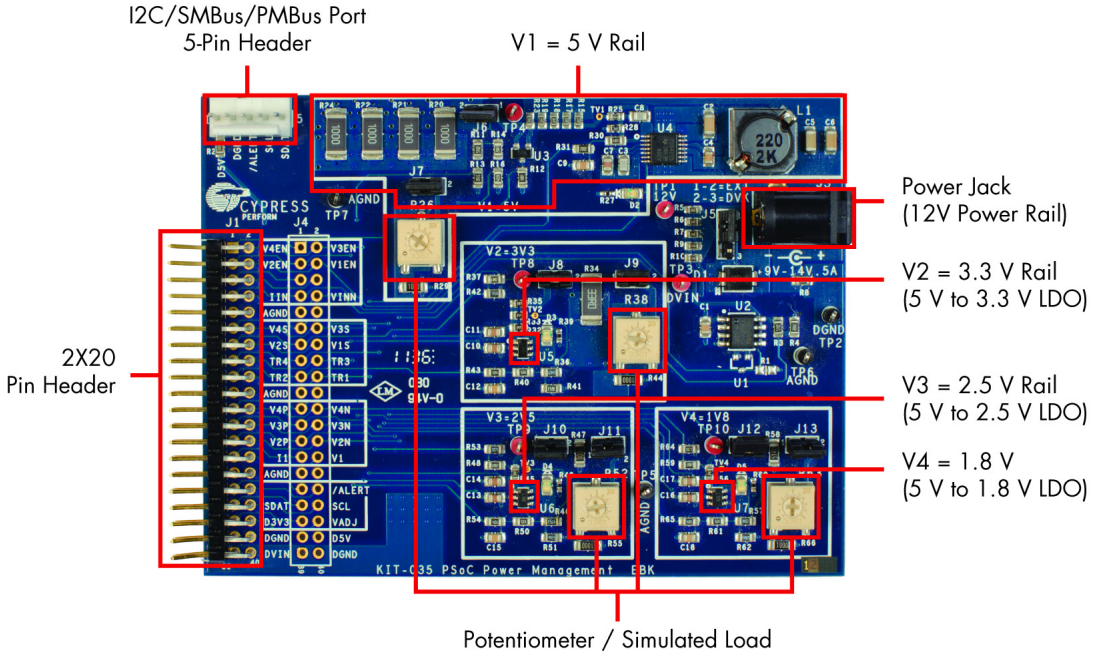
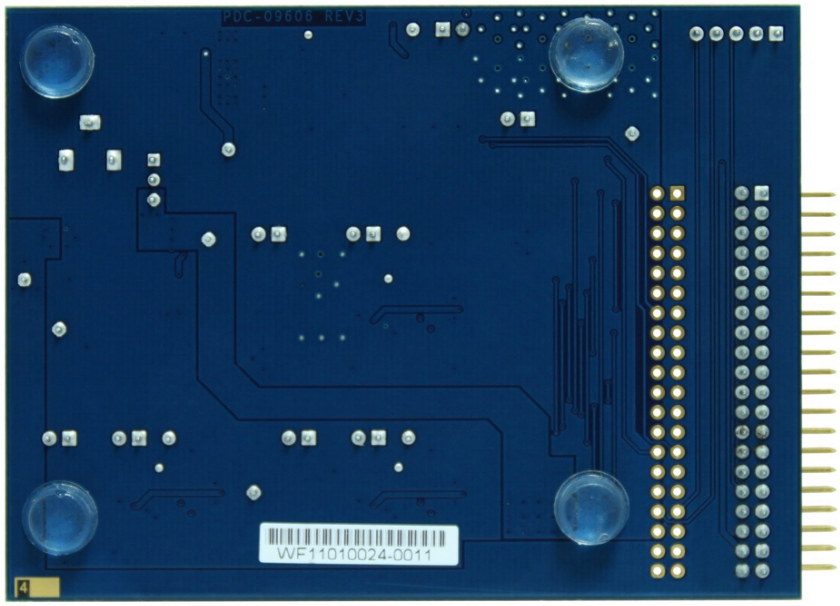


Figure 4-3. Power Supervision EBK PCB (Bottom)



4.3 Headers and Jumpers

A number of headers and jumpers are provided on the Power Supervision EBK. Table 4-1 outlines the function of each item and the default configuration.

Table 4-1. Power Supervision EBK Jumper Settings

PCB Designator	Description	Factory Default Configuration
J1	2×20 pin header to connect to the PSoC Kit	–
J2	5-pin header to connect an external host or management processor via I2C/ SMBus/PMBus	–
J3	Power jack	–
J4	2×20 pin header that replicates signals on J1 for easy connection to a logic analyzer or oscilloscope	–
J5	3-pin header for primary input power source selection. Place the jumper in 1-2 position to source power from the DC power jack J3. Place the jumper in 2-3 position to source power from the PSoC platform kits	2-3 position
J6	2-pin header to connect all loads on V1 = 5-V rail (this includes the fixed and adjustable loads on V1, as well as the load presented by the V2, V3, and V4 rails)	Installed
J7	2-pin header to connect the potentiometer load on V1 = 5-V rail	Installed
J8	2-pin header to connect all loads on V2 = 3.3-V rail (fixed and adjustable)	Installed
J9	2-pin header to connect the potentiometer load on V2 = 3.3-V rail	Installed
J10	2-pin header to connect all loads on V3 = 2.5-V rail (fixed and adjustable)	Installed
J11	2-pin header to connect the variable potentiometer on V3 = 2.5-V rail	Installed
J12	2-pin header to connect all loads on V4 = 1.8-V rail (fixed and adjustable)	Installed
J13	2-pin header to connect the variable potentiometer on V4 = 1.8-V rail	Installed

4.4 2x20 Pin Interface Header

The following table outlines the definition of the 40-pin J1 header interface.

Table 4-2. 2×20 Header (J1) Pin Definition

Description	Signal	Pin	Pin	Signal	Description
Voltage Regulator 4, Enable	V4EN	1	2	V3EN	Voltage Regulator 3, Enable
Voltage Regulator 2, Enable	V2EN	3	4	V1EN	Voltage Regulator 1, Enable
–	NC	5	6	NC	–
Power Rail Current (measured as single-ended voltage)	IIN	7	8	VIN	Power Rail Sensing Voltage
Analog Ground	AGND	9	10	NC	–
Voltage Regulator 4, Fault Sensing Voltage	C4	11	12	C3	Voltage Regulator 3, Fault Sensing Voltage
Voltage Regulator 2, Fault Sensing Voltage	C2	13	14	C1	Voltage Regulator 1, Fault Sensing Voltage
Voltage Regulator 4, Trim	TR4	15	16	TR3	Voltage Regulator 3, Trim
Voltage Regulator 2, Trim	TR2	17	18	TR1	Voltage Regulator 1, Trim
Analog Ground	AGND	19	20	NC	–
Voltage Regulator 4, Current (measured as differential voltage)	I4	21	22	V4	Voltage Regulator 4
Voltage Regulator 3, Current (measured as differential voltage)	I3	23	24	V3	Voltage Regulator 3
Voltage Regulator 2, Current (measured as differential voltage)	I2	25	26	V2	Voltage Regulator 2
Voltage Regulator 1 Current (measured as single-ended voltage)	I1	27	28	V1	Voltage Regulator 1
Analog Ground	AGND	29	30	NC	–
–	NC	31	32	/ALERT	Alert Signal (I2C/SMBus/PMBus)
Serial Data (I2C/SMBus/PMBus)	SDAT	33	34	SCL	Serial Clock (I2C/SMBus/PMBus)
Unused	D3V3	35	36	VADJ	Unused
Digital Ground	DGND	37	38	D5V	Unused
Optional 12-V power from PSoC Kit/PSoC 3 Kit/PSoC 5LP Kit	DVIN	39	40	DGND	Digital Ground

5. Example Projects

5.1 Example Project 1: Advanced Sequencer

5.1.1 Overview

This example demonstrates the following features:

- Voltage sequencing
- Under-voltage (UV) and over-voltage (OV) monitoring using the window comparator for rapid fault detection

If the project is running correctly, all four green LEDs on the Power Supervision EBK are turned on and debug information appears on the LCD display, as shown in Figure 5-1.

Figure 5-1. Example 1 - LCD Display for Normal Operation

The four digits indicate the rail failure status (UV or OV). A dash '–' indicates that the rail is within defined operating limits (± 10 percent of nominal voltage). If there is a failure on any rail, the rail number will be displayed next to the UV or OV indicator. For example, if you remove jumper J6, then you will remove power to regulators 2 through 4. This causes a UV fault on rails 2 through 4 and the display appears, as shown in Figure 5-2. Note that depending on when you remove the jumper, the failure may not be detected on all three rails simultaneously. To verify correct operation of both UV and OV fault detection on each rail, consider shorting the C1, C2, C3, and C4 pins in the J4 connector on the Power Supervision EBK to ground or to the 5-V rail output (TP4).

Figure 5-2. Example 1 - LCD Display with J6 Removed

Also, the Voltage Sequencer component is configured to shut down all rails on any fault condition, so the four green LEDs on the Power Supervision EBK should turn off when jumper J6 is removed. The Voltage Sequencer component is configured to automatically re-sequence all rails in response to a fault. Note that if jumper J6 is not placed back, a timeout fault occurs on rail 2 (not repeated on LCD). When the fault occurs, only the LED for rail 1 and rail 2 are ON. Due to this, you might observe a flashing pattern for these two LEDs.

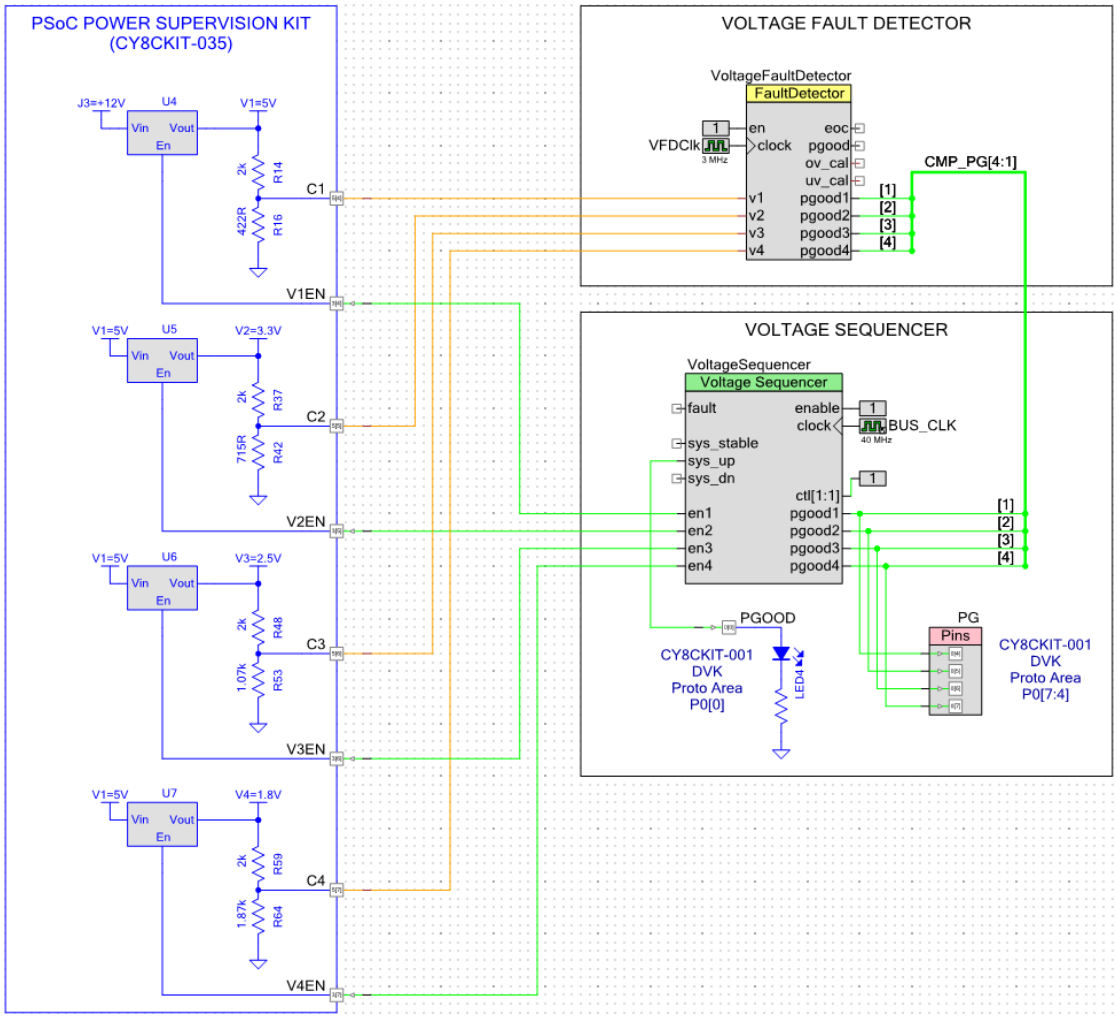
In the PSoC kit, when all rails are powered, an LED turns on. The LED turns off if any of the rails are not powered due to a fault.

5.1.2 Technical Details - Voltage Sequencing

The Voltage Sequencer component enables designers to control both the power-up and power-down sequence and timing of up to 32 secondary-side voltage supplies. It is designed to connect to regulators that provide a digital power good (PGOOD) status output. In this example project, the

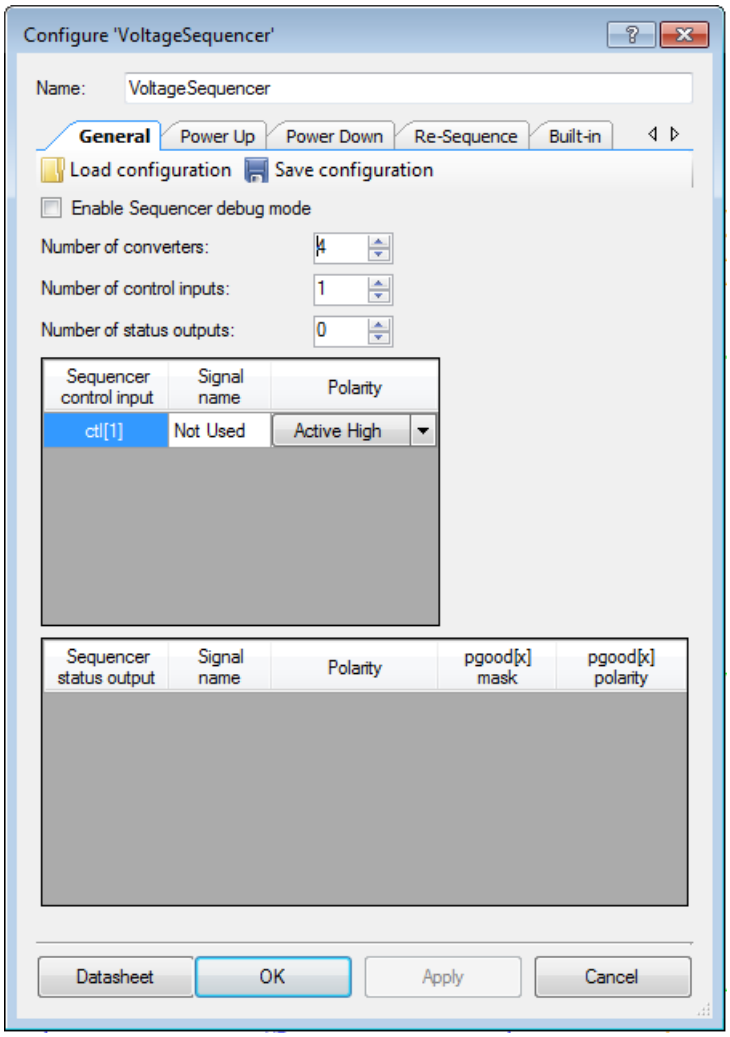
regulators on the Power Supervision EBK are monitored using the under-voltage/over-voltage window comparator logic inside PSoC with programmable thresholds on each rail. This generates equivalent PGOOD signals internally that connect to the Voltage Sequencer component (see Figure 5-3).

Figure 5-3. Advanced Sequencer Architecture



To see the configuration of the sequencer, double-click **Voltage Sequencer** in the Example 1 top-level design schematic file. This opens the component customizer for the Voltage Sequencer. The General tab is displayed by default (see Figure 5-4).

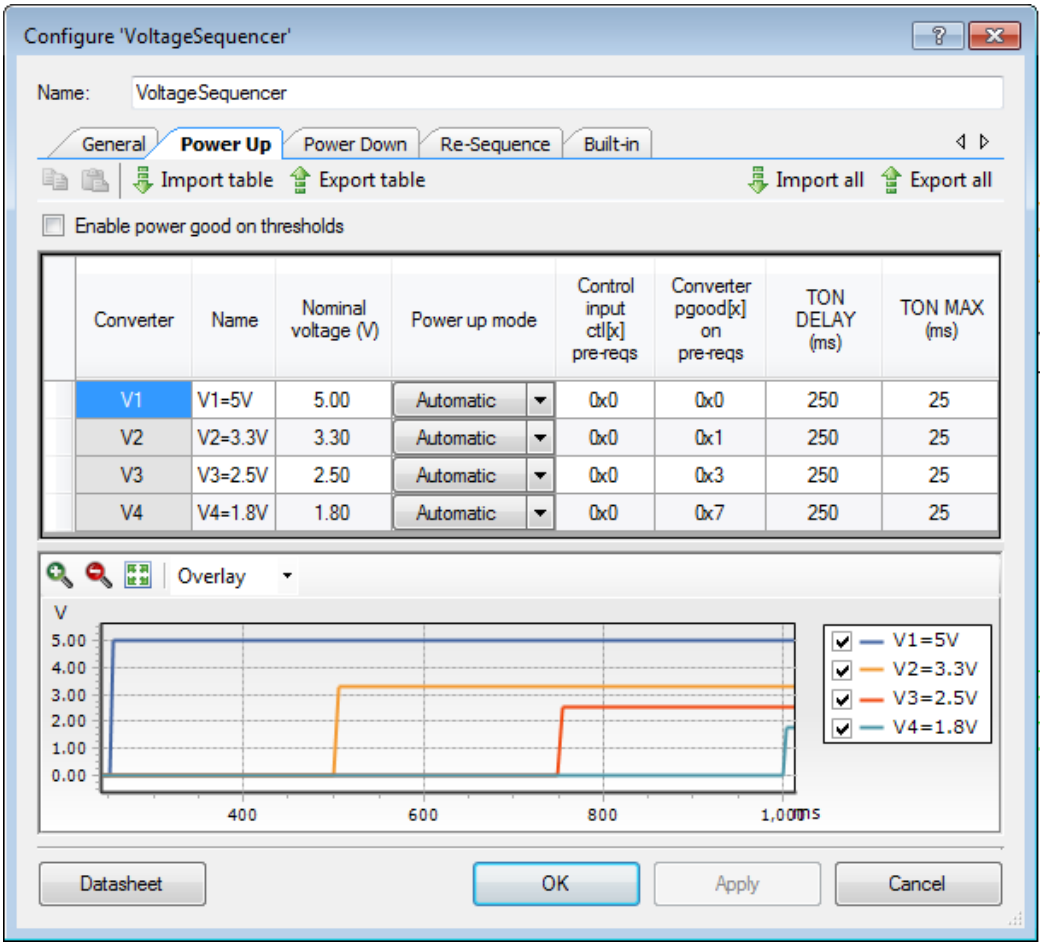
Figure 5-4. Voltage Sequencer Customizer General Tab



For this example project, the key parameter setting is the number of converters. This should be set to four to match the number of regulators on the Power Supervision EBK.

Click the **Power Up** tab to set up the power-up sequence for this example (see Figure 5-5).

Figure 5-5. Voltage Sequencer Customizer Power Up Tab



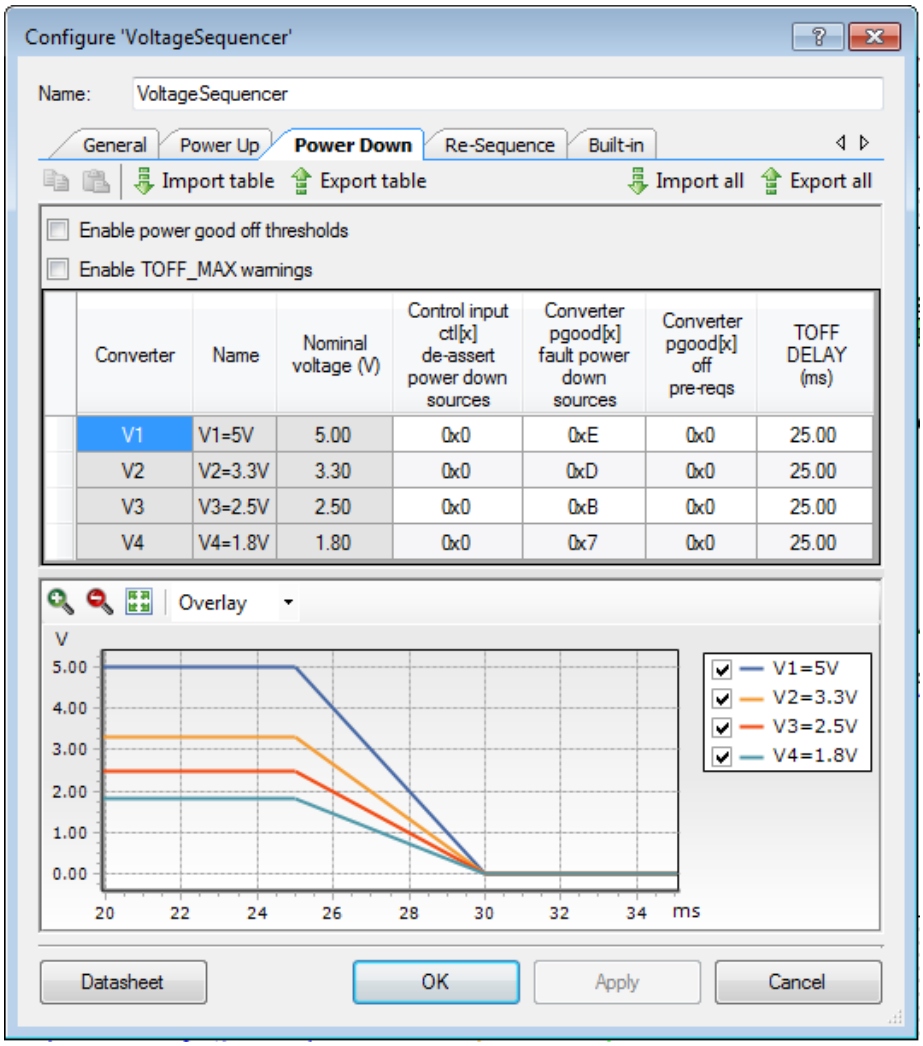
The sequence order can controlled through the *Converter pgood[x] pre-reqs* parameter. When a bit is set in this field, the rail cannot begin sequencing until the selected rails are powered up. For example, the entry for V2 is 0x01. This means rail 2 cannot begin sequencing until rail 1 is powered up. Clicking that parameter pops up a dialog to convert the desired rail prerequisites to a hexadecimal number. Because rails 2 through 4 derive their input power from the output of regulator 1 (this is a hard-wired connection on the Power Supervision EBK), you must power up rail 1 first. Therefore, V1 can never have a pgood prerequisite when working with the Power Supervision EBK.

The *TON DELAY* parameter specifies the sequence timing. It is the delay that is executed from the moment the prerequisite conditions for that rail (other rail pgoods in this case) are met until the rail is enabled for the first time. All rails have this parameter set to 250 ms and rails 2 to 4 are configured to wait for previous rails to power-up before they begin sequencing. This results in a 250-ms delay between all four rail enables, as shown in the waveform graphic on this tab. You can reconfigure the power-up sequence of the other three rails (V2 through V4).

The *TON MAX* parameter defines how long the Voltage Sequencer can wait after enabling a regulator before its pgood input is asserted. If pgood is asserted sooner than this time-out period, then the rail is declared good. Otherwise, it is considered a fault condition.

Click the **Power Down** tab to set up the power-down sequence for this example (see Figure 5-6).

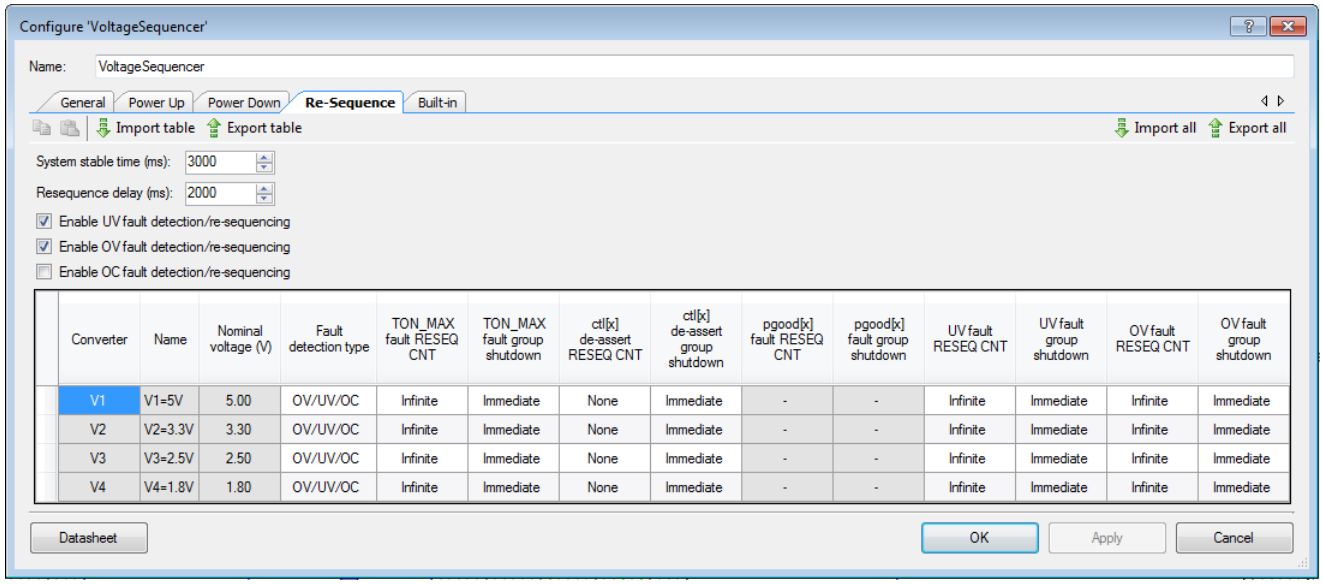
Figure 5-6. Voltage Sequencer Customizer Power Down Tab



The *Converter pgood[x] fault power down sources* parameter specifies whether the regulator should turn off in case of a fault on another rail. This is useful when multiple regulators power the same chip or subsystem. The *TOFF DELAY* parameter sets the power-down timing for the system. Because all parameters have been set to 25 ms, all rails will turn off at the same time. The chart in the lower part of this tab displays the current sequencer configuration to confirm that the settings are entered correctly.

Finally, click the **Re-sequence** tab to configure automatic re-sequencing options. The three relevant fault conditions applicable to this example are TON MAX, UV Fault, and OV Fault. It is possible to specify different re-sequencing options depending on the fault type, but in this example the Voltage Sequencer is configured to turn off the rail group immediately (ignoring the *TOFF Delay* parameter) and it will attempt to re-sequence indefinitely in response to any fault condition (see Figure 5-7)

Figure 5-7. Voltage Sequencer Customizer Re-sequence Tab

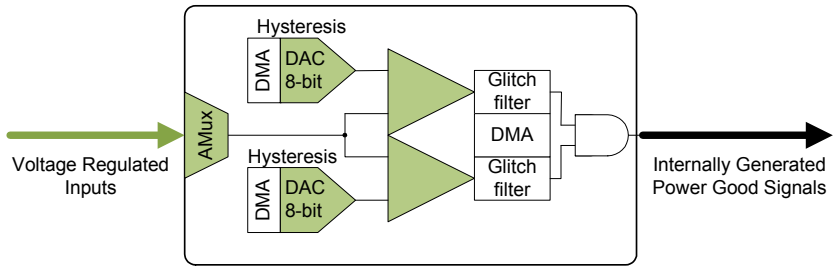


5.1.3 Technical Details - UV/OV Monitoring using the Window Comparator

To support over-voltage and under-voltage detection on the four secondary power supply rails, eight comparators and eight programmable DACs are required. As the number of regulators in the systems expands, the number of comparators and DACs required becomes excessive. To make efficient use of analog hardware resources, an alternative implementation has been implemented as illustrated in Figure 5-8.

A single window comparator and glitch filter are rapidly time-multiplexed across all the rails requiring monitoring (see Figure 5-8). Note the use of DMA controllers to control the UV/OV DACs and the glitch comparator circuits. The DMA controllers inside PSoC are extremely versatile and can transfer between SRAM, peripherals, and nonvolatile flash memory in any combination. Because the window comparator performs a time-critical fault detection function, it is desirable to have that block function with zero interaction with the CPU. The DMA controllers make that happen.

Figure 5-8. Time Multiplexed Over/Under-Voltage Detection Hardware



Time Multiplexed Window Comparator and Glitch Filter

The time-multiplexing works according to this sequence:

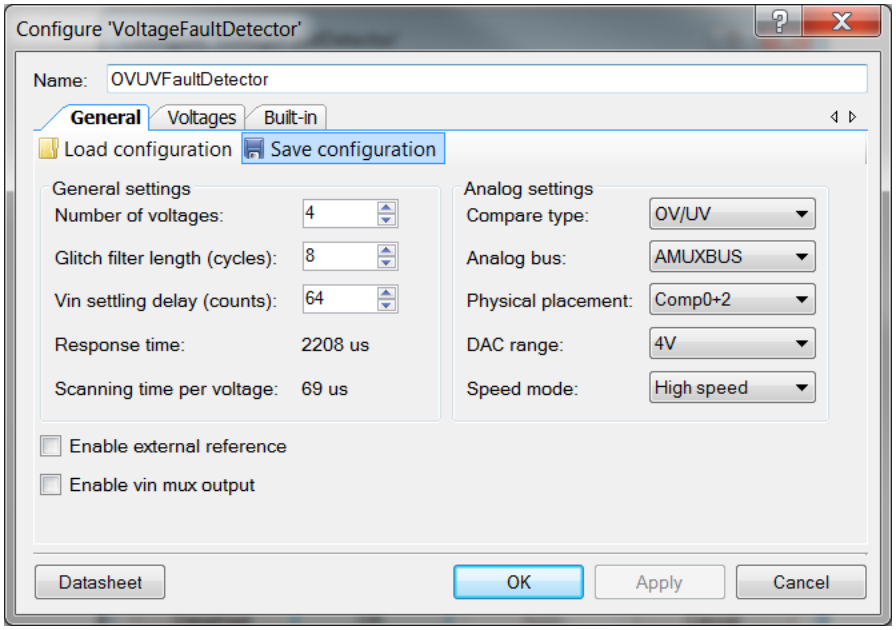
1. The scaled regulator output for rail[n] (signal V[n]) is multiplexed into the window comparator
2. The UV and OV limits for rail[n] are copied from SRAM to the DAC using DMA
3. The previous glitch filter result for rail[n] is copied from SRAM to the glitch filter using DMA
4. A short delay is provided to allow the DACs and comparators time to settle

5. The comparator OV and UV results are sampled by the glitch filters
6. The current glitch filter result for rail[n] is copied back to SRAM using DMA
7. Connection to rail[n] (signal V[n]) is removed
8. The next rail[n+1] (signal V[n+1]) is selected and steps 1 to 7 repeat for that rail

On the Power Supervision EBK, the four secondary regulator output voltages (signals C[4:1]) are all normalized to about 1 volt using scaling resistors. This makes it possible to use the internal DAC's fastest update rate of 1,000 ksps using the 1 volt range (the DAC's 4-V range update rate is 250 ksps). Scaling the input voltage gives the best possible performance. If higher speed is not required for your application and all the secondary rails in your system are lower than 4 V (the maximum DAC range), scaling of the regulator outputs can be eliminated.

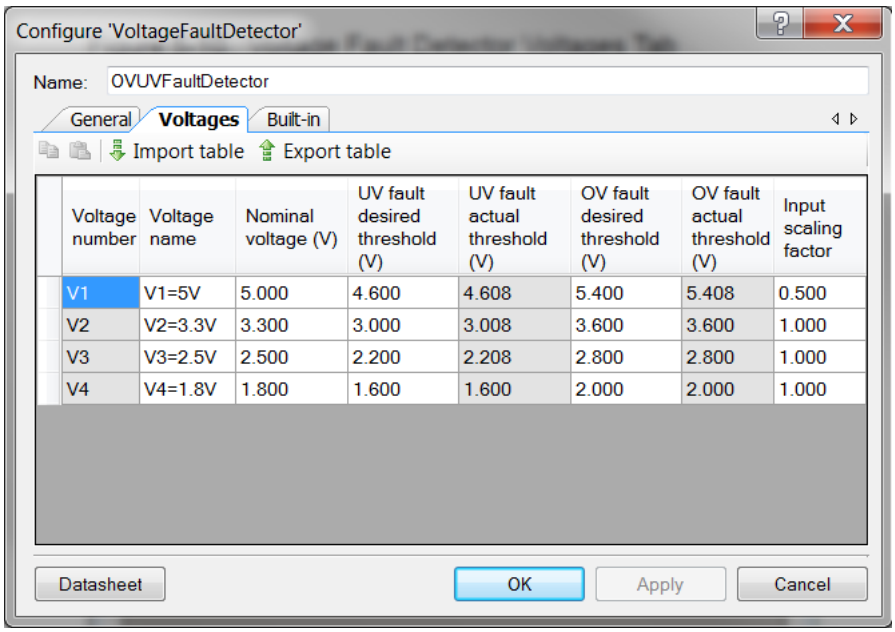
To see the configuration of this component, double-click **Voltage Fault Detector** in the Example 1 top-level design schematic file. This opens the component customizer and the General tab is displayed by default (see Figure 5-9).

Figure 5-9. Voltage Fault Detector Customizer General Tab



For this example project, the key parameter settings are the Number of voltages (4), and the Compare type (OV and UV). Click the **Voltages** tab to set up the fault thresholds for this example (see Figure 5-10).

Figure 5-10. Voltage Fault Detector Voltages Tab



Voltage number	Voltage name	Nominal voltage (V)	UV fault desired threshold (V)	UV fault actual threshold (V)	OV fault desired threshold (V)	OV fault actual threshold (V)	Input scaling factor
V1	V1=5V	5.000	4.600	4.608	5.400	5.408	0.500
V2	V2=3.3V	3.300	3.000	3.008	3.600	3.600	1.000
V3	V3=2.5V	2.500	2.200	2.208	2.800	2.800	1.000
V4	V4=1.8V	1.800	1.600	1.600	2.000	2.000	1.000

For each rail, the nominal voltage, under-voltage and over-voltage thresholds can be entered. The Input scaling factor parameter enables you to enter the scaling used externally to attenuate the C[n] inputs to below 1 V.

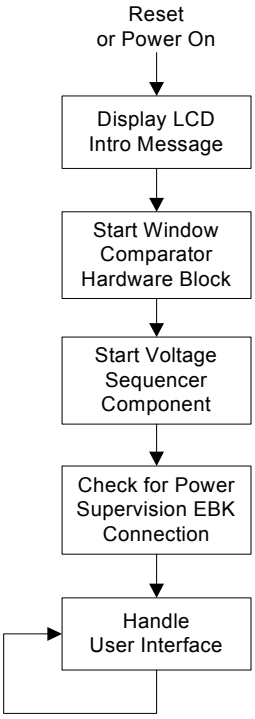
5.1.4 Technical Details - Firmware Flowchart

The Voltage Fault Detector component is entirely hardware driven after it is initialized. This frees the CPU core completely for other application-specific user tasks. In the Example 1 project, the user task is updating the LCD display.

The Voltage Sequencer component is firmware driven and is triggered by an interrupt every 250 µs to service potential changes. Fault response handling has a separate interrupt handler to enable timely response to fault conditions. The fault handler interrupt service routine (ISR) is primarily responsible for turning off non-faulty rails in response to a faulty rail as defined by the *Converter pgood[x] fault power down sources* parameter on the Power Down tab. Note that turning off a rail that has a fault condition (its own pgood signal being de-asserted) is handled entirely in hardware to get the fastest possible response time (~25 ns) for safety reasons.

The firmware flowchart for the Example 1 project is shown in Figure 5-11.

Figure 5-11. Example 1 Firmware Flowchart



5.2 Example Project 2: Power Supervision

5.2.1 Overview

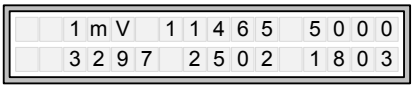
This example builds on the Example 1 project and demonstrates a much more comprehensive power supervision solution with the following features:

- Power supply sequencing
- Power supply voltage and current measurement accurate to 0.26 percent
- Power supply trimming accurate to better than 0.6 percent
- Power supply over-voltage and under-voltage fault detection using window comparators
- PSoC Power Supervision Tool for monitoring voltage and current

The PSoC Power Supervision Tool is standalone GUI software that enables you to configure and interact with Cypress Power Supervision Solutions over the PMBus interface. Besides monitoring the voltage and current, it can also control the state of the rails.

If the project is running correctly, all four green LEDs on the Power Supervision EBK should be turned on and voltage measurements appear on the LCD display, as shown in Figure 5-12.

Figure 5-12. Example 2 - LCD Display with Voltage Measurements

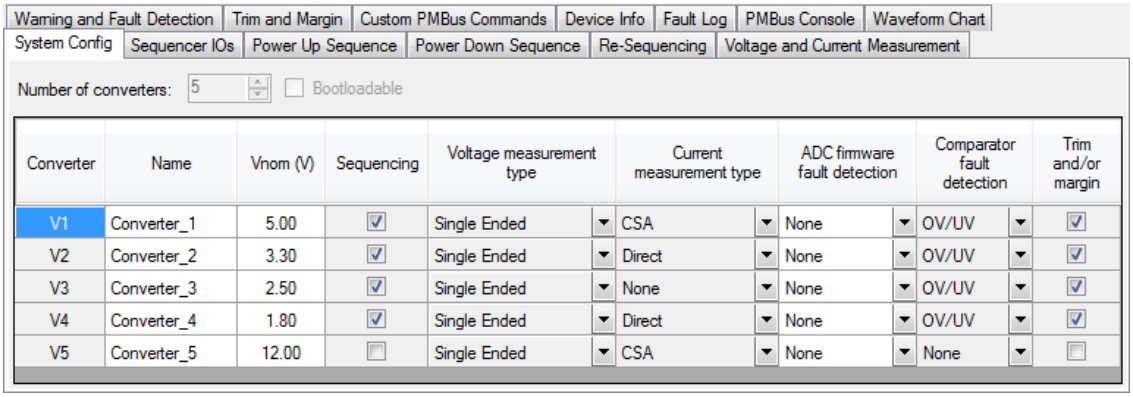


The PSoC Power Supervision Tool should automatically find and connect to the MiniProg3. If it does not (if more than one MiniProg3 are connected to your PC), select the appropriate MiniProg3 and click **Connect**. The indicators should display ‘Connected’ and ‘Powered On’, and they should turn

green. After the PSoC Power Supervision tool is connected, click **Read All**. The system-level settings is loaded from the PSoC device in the **System Config** tab. This tab provides a snapshot of the Power Supervision configuration programmed on PSoC – in this case, the Example Project 2 for the CY8CKIT-035.

The System Config tab should appear as shown in Figure 5-13. V1 to V4 are the four secondary rails associated with the power converters on the CY8CKIT-035, and V5 is the primary (+12 V) input power rail.

Figure 5-13. PSoC Power Supervision Tool - System Config Tab



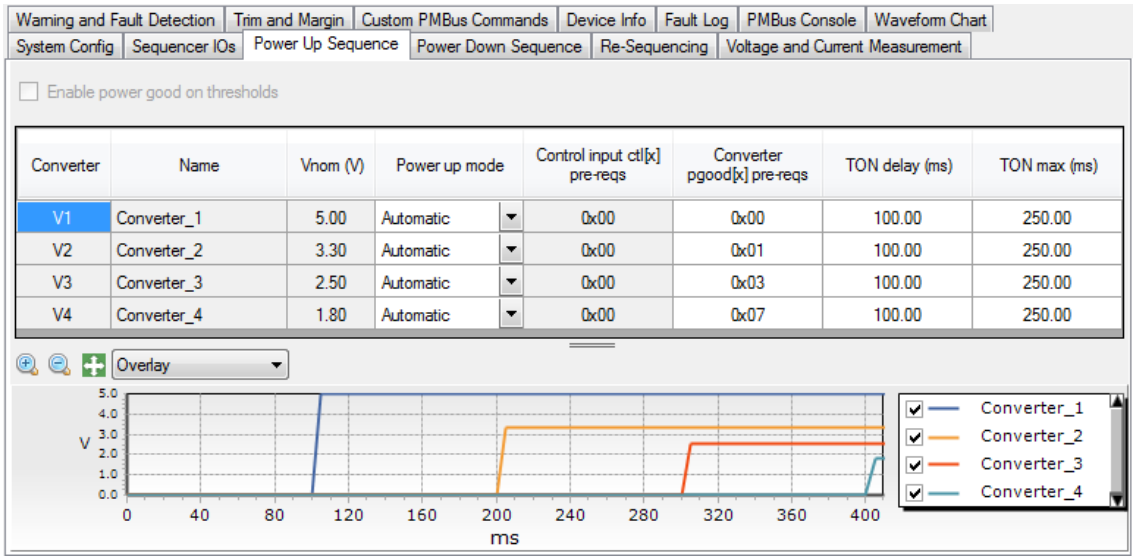
As you can see, functions such as sequencing, voltage and current measurement, over-voltage and under-voltage fault detection, and trimming are enabled for converter rails V1 to V4. As the primary input power rail, V5 cannot be sequenced or trimmed.

Voltage measurement type is set to single-ended for all rails. An external CSA is used for current measurements on rails V1 and V5. Current is directly measured across a shunt resistor for rails V2 and V5. Rail V3 does not support current measurement.

5.2.2 Technical Details - Voltage Sequencer and UV/OV Fault Detection

The voltage sequencer and under-/over-voltage window comparator circuits are fundamentally similar to that of Example 1. To change any parameter in the sequencing, click the **Power Up Sequence** tab of the PSoC Power Supervision Tool. This tab enables you to specify how the voltage sequencer should power up the rails.

Figure 5-14. PSoC Power Supervision Tool - Power Up Sequence Tab



Note: Rail V5 is not sequenced because it is the primary rail.

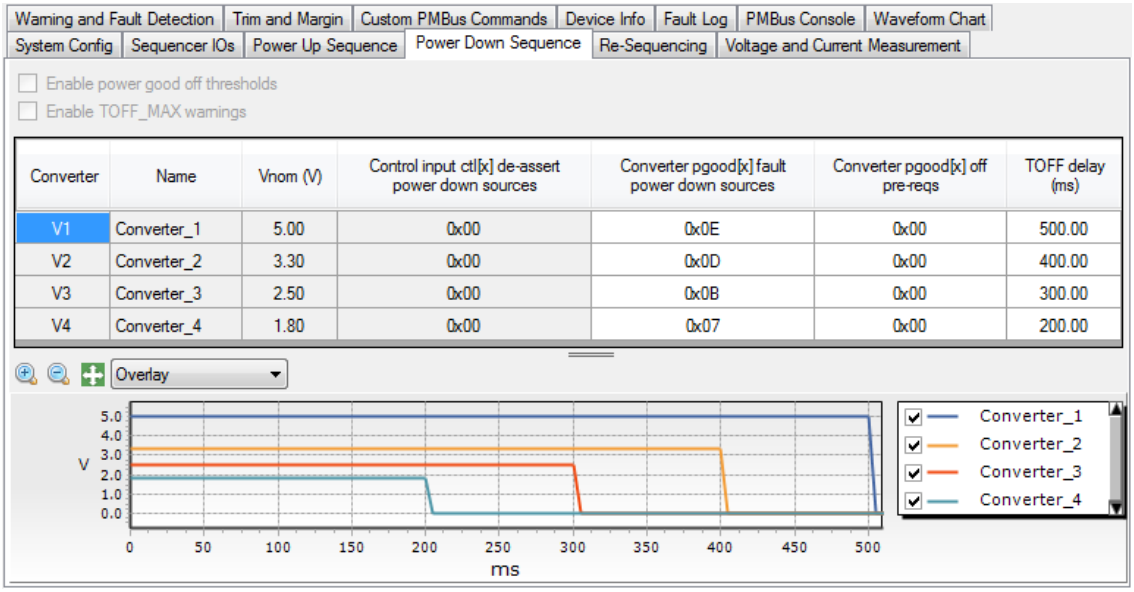
The **Converter pgood[x] pre-reqs** parameter defines the prerequisites of each rail based on the PGOOD input signal in the voltage sequencer. The PGOOD signal is only HIGH when the rail has reached nominal voltage and is stable.

Every rail has two timing parameters associated with the powering up.

- The **TON DELAY** parameter specifies how much time to wait after the rail's prerequisite conditions become true before enabling the power converter by asserting its EN signal.
- The **TON MAX** parameter specifies the acceptable time limit for the power converter to ramp up to nominal voltage after it is enabled. The ramp-up time is defined as the time between EN signal being asserted and the PG signal to go active HIGH. If the ramp-up time exceeds the TON MAX parameter, a fault occurs.

To change the sequencing down, click the **Power Down Sequence** tab of the Power Supervision Tool. This tab enables you to specify how the Voltage Sequencer should power down the rails.

Figure 5-15. PSoC Power Supervision Tool - Power Down Sequence Tab



The **Converter pgood[x] fault power down sources** allows you to specify which good rails belong to the same group as the faulty rail and therefore, should also be powered down. In the example project, if any rail is faulty, all rails will power down.

The **Converter pgood[x] off pre-reqs** allows you to define a power-down sequence. A converter will not power down until all of the specified prerequisite converters have successfully powered down. In the example project, there is no dependency among the rails when powering down.

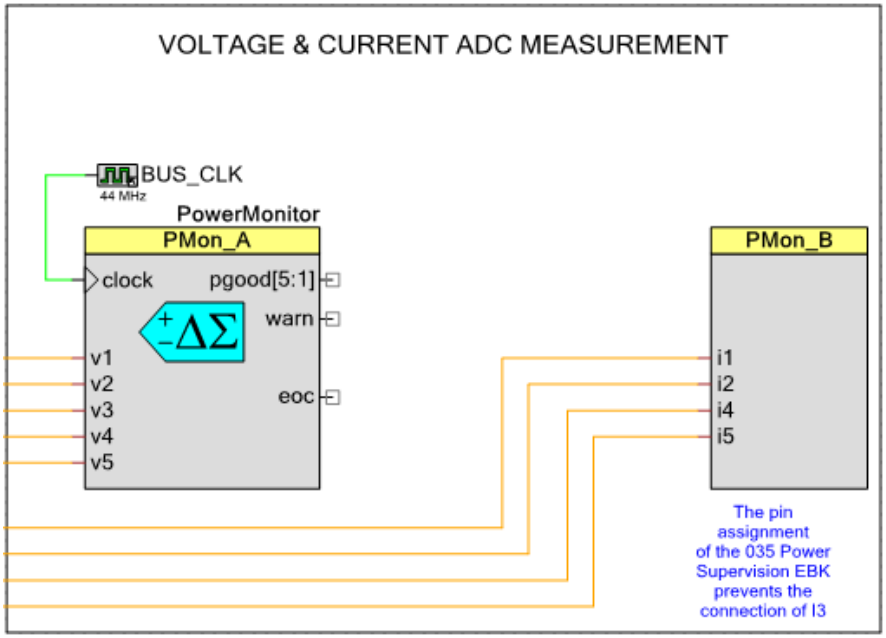
The **TOFF DELAY** parameter specifies how much time to wait after a power down is initiated and before the EN of the associated power converter is deasserted.

To change voltage threshold limits for fault detection, click the **Warning and Fault Detection** tab of the Power Supervision Tool. This tab lets you specify the OV and UV warning/fault threshold limits.

5.2.3 Technical Details - Voltage and Current Measurements

In Example 2, voltage rail voltage and current measurements use the differential 12-bit Delta-Sigma ADC with 0.1 percent internal accurate voltage reference, with automatic self-calibration resulting in a system-level accuracy of 0.26 percent. Figure 5-16 shows the Power Monitor component in the Top Design.

Figure 5-16. Power Monitor Component

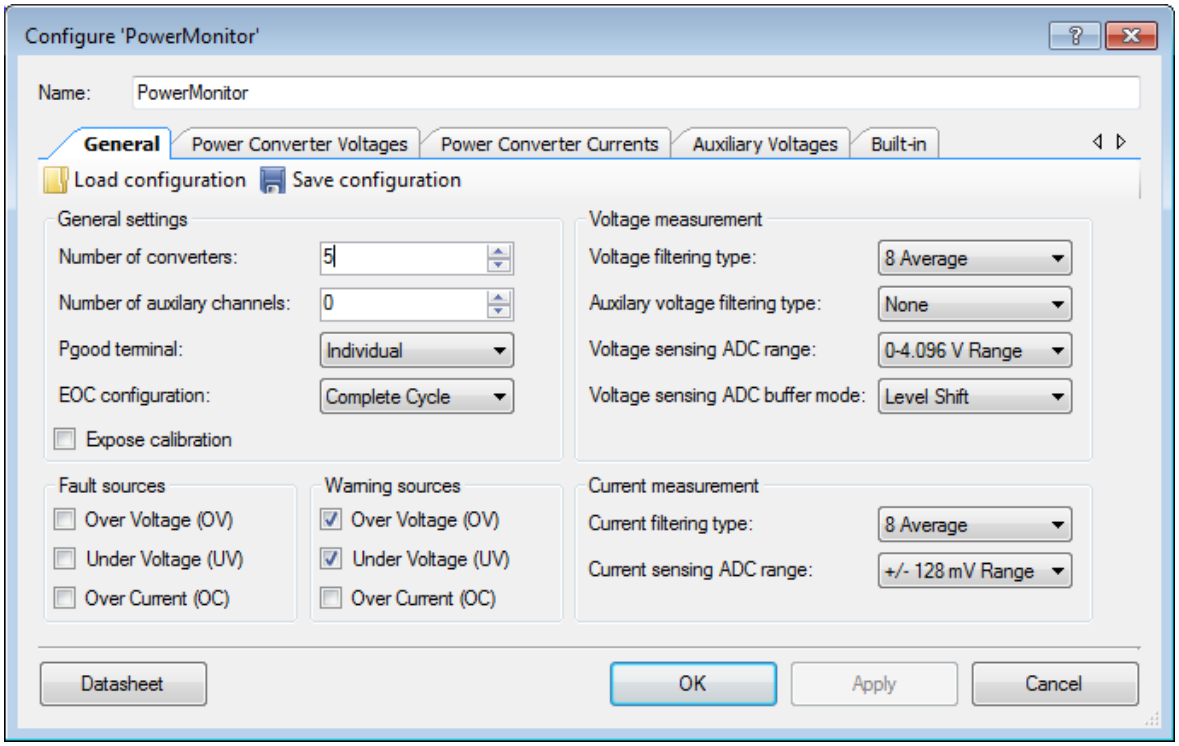


To measure voltages, the Delta-Sigma ADC is configured to use a ±2048-mV input range with a 2048-mV reference (generated by doubling the internal 1024-mV reference) on the inverting input terminal, yielding an actual single-ended voltage measurement range of 0 to 4096 mV. This range is used to measure the voltages of each of the regulator rails on the Power Supervision EBK. For rails V2 = 3.3 V, V3 = 2.5 V, and V4 = 1.8 V, those voltages are compatible with the ADC setting and can be directly connected to PSoC (V2, V3, and V4 in Figure 5-16). For V1 = 5 V and the primary 12-V input, the voltages are scaled using external resistors to make them compatible with the ADC input voltage range at the expense of some additional measurement inaccuracy caused by the tolerances of the external resistors used (VIN and V1 in Figure 5-16).

Two different methods are used for current measurement, also depending on the voltage level of the regulator output. For rails V2 = 3.3 V, V3 = 2.5 V, and V4 = 1.8 V, a high-side shunt resistor is placed in series with the regulator output. The differential voltage developed across that resistor is directly proportional to load current. To support that measurement, the ADC configuration is dynamically changed to a ± 128-mV range. To minimize voltage loss and power dissipation, the resistance value is chosen to be as low as possible and should have 0.1-percent tolerance to maintain overall system measurement accuracy of 0.26 percent. For V1 = 5 V and the primary 12-V input, the current shunt resistor method cannot be used directly. Attempting to scale both sides of the current shunt resistor to a lower voltage range adds error to the measurement that is difficult to calibrate out. For those rails, the Power Supervision EBK uses low-cost external current sense amplifiers (such as the Zetex ZXCT1009 or Maxim 4080), that convert the differential voltage across the shunt resistor to a single-ended voltage compatible with the ADC input voltage range.

To see the configuration of the **Power Monitor** component, double-click it in the Example 2 top-level design schematic file. This opens the component customizer and the General tab is displayed by default (see Figure 5-17).

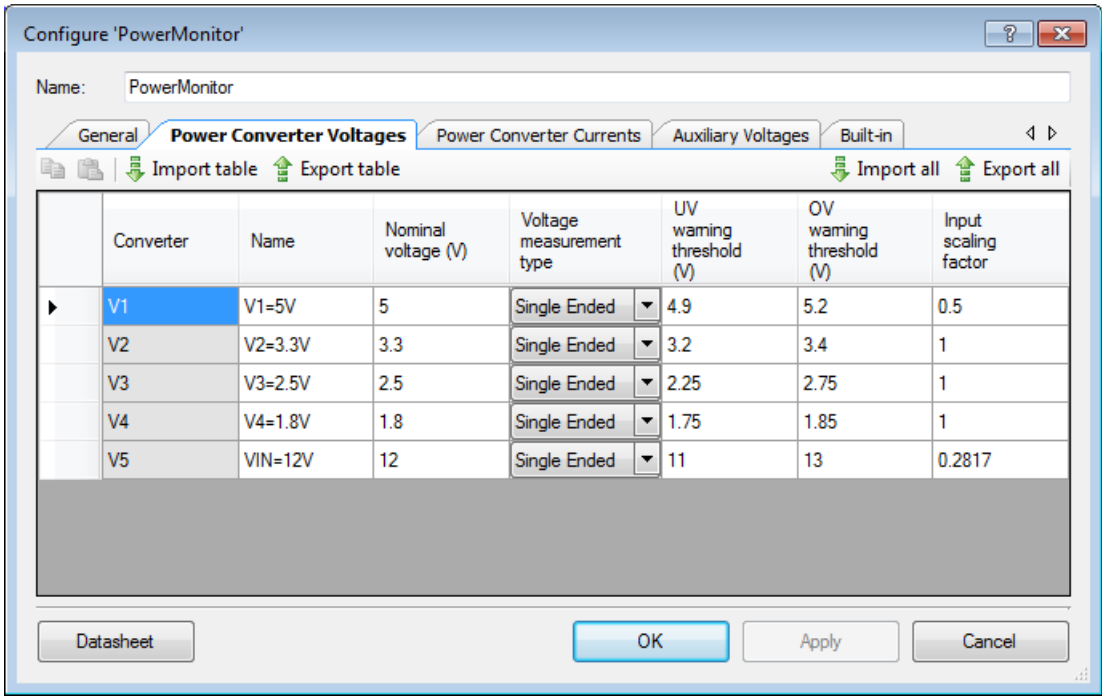
Figure 5-17. Power Monitor General Tab



For this example project, the key parameter settings are the number of converters (five including the 12-V primary input), the current sensing ADC range (±128 mV to be compatible with the Power Supervision EBK), the voltage sensing ADC range (0–4.096 V to work with 5-V Vdd).

Click the **Power Converter Voltages** tab to set up voltage measurements for this example (see Figure 5-18).

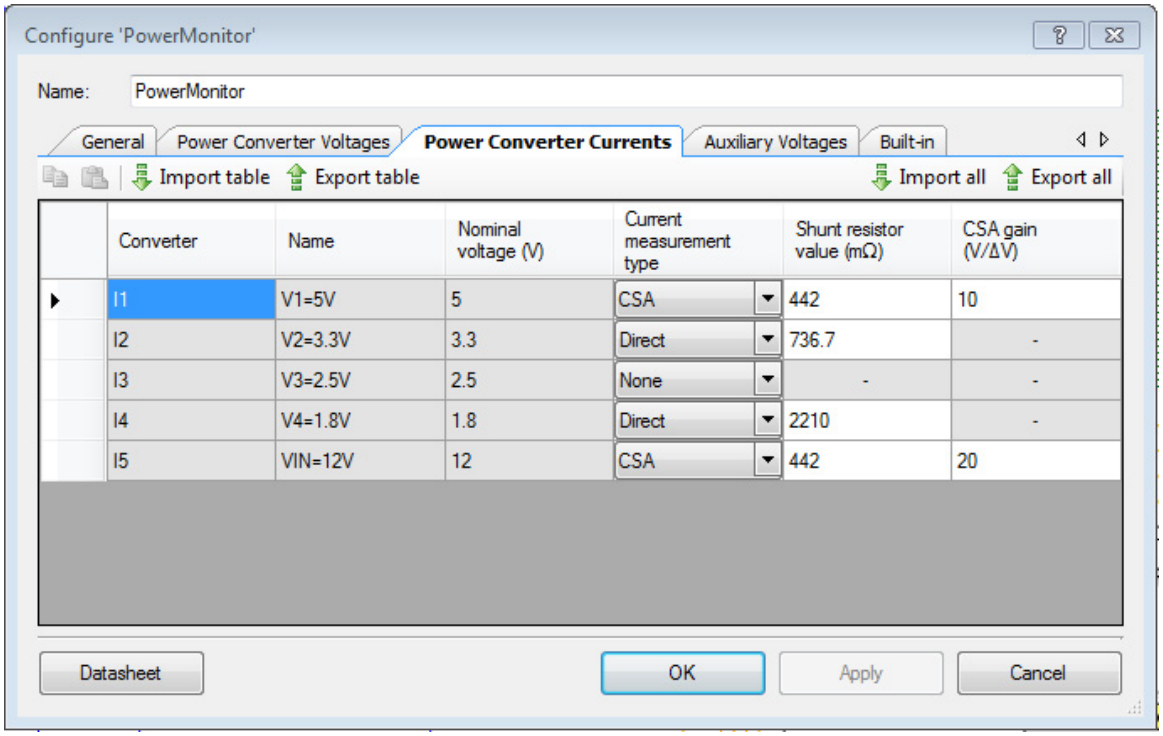
Figure 5-18. Power Monitor Power Converter Voltages Tab



In this tab, you can set nominal voltages, voltage measurement type (Single Ended or Differential), under-voltage and over-voltage warning, and fault thresholds as well as the input scaling factor, similar to that same parameter for the Voltage Fault Detector component in Example 1. All of these settings are selected to match the Power Supervision EBK.

Click the **Power Converter Currents** tab to set up current measurements for this example (see Figure 5-19).

Figure 5-19. Power Monitor Power Converter Currents Tab



In this tab, you can set the current measurement type (Current Sense Amplifier, Direct or None), over-current warning and fault thresholds, as well as parameters related to the current sensing hardware. The series shunt resistor value field cannot be left blank. Similarly, the CSA gain factor must be specified when CSA current measurement type is selected for a rail. All of these settings are selected to match the Power Supervision EBK.

ADC conversion time depends on several factors including the CPU clock frequency inside PSoC, the resolution of the ADC and the time taken to switch inputs and change ADC configuration. At a CPU clock frequency of 44 MHz (as used in Example 2), the time taken to execute those fundamental tasks is outlined below:

- Using the ±2048-mV range: 53 µs per reading
- Changing to ±128-mV range: 320 µs
- Using the ±128-mV range: 70 µs per reading
- Changing to ±2048-mV range: 320 µs

You can also view the power monitoring settings by clicking the **Voltage and Current Measurement** tab of the Power Supervision tool. None of these settings are editable when using the tool.

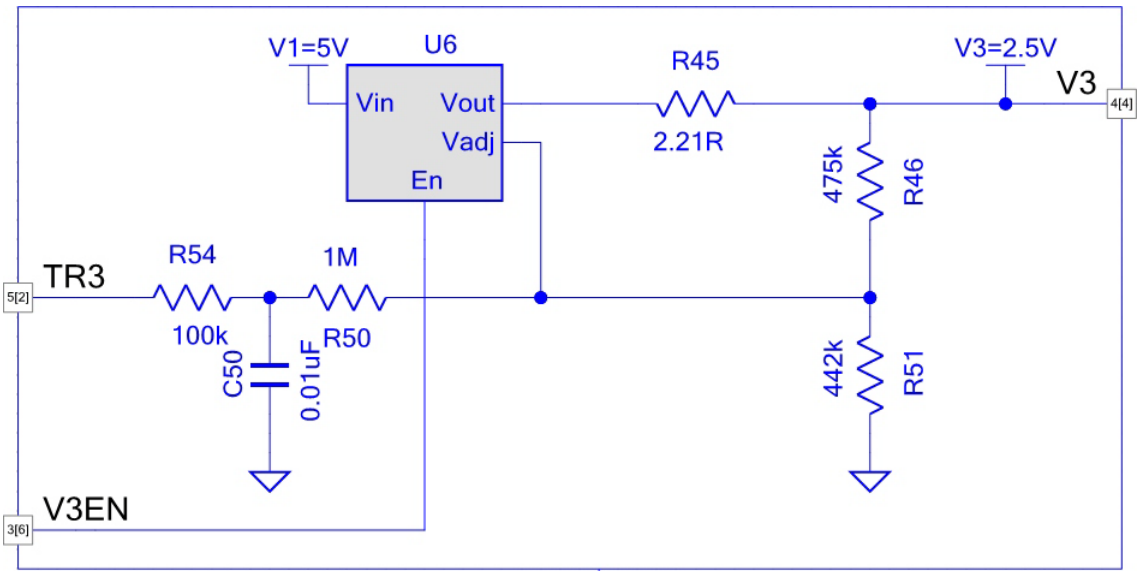
5.2.4 Technical Details - Regulator Trimming and Margining

Trimming (fine-tuning) of each regulator output is achieved by applying a controlled analog voltage to the "feedback" (V_{FB}) or "adjust" (V_{ADJ}) analog control pin on the regulators. Trimming the four secondary power supply rails requires four additional DACs to the ones already being used for the under-/over-voltage window comparator circuit. As the number of regulators in the systems expands, the number of DACs required for trimming and margining becomes excessive. To make more efficient use of analog hardware resources, an alternative implementation is developed based on PWM blocks with external RC filter networks to achieve the equivalent result. Because PSoC can measure the analog voltage of each rail, a closed loop control system can be implemented to fine-

tune each regulator output beyond the accuracy specifications of the regulators themselves. This is known as “active trimming”.

The circuit in Figure 5-20 shows the details of the trimming/margining circuit for V3 = 2.5-V rail. The output scaling network of R46 and R51 are the recommended values provided by the regulator manufacturer to ensure that the regulator can sense its own output voltage and regulate it as the load varies. The TR3 pin is a PWM output signal from PSoC that gets filtered by R54/C15 and that voltage is summed into the FB pin of the regulator through R50. If the PWM duty cycle controlled by PSoC is reduced, the voltage applied to the Vadj will reduce and the regulator will respond by increasing its output voltage. Conversely, if the PWM duty cycle is increased, the voltage applied to the Vadj pin will increase and the regulator will respond by decreasing its output voltage. Typical power supplies respond in this manner; for others that do not, this circuit both internal to PSoC and external can be customized for the specific power supply chosen (for example: inverting the PWM output such that a decrease in PWM duty cycle decreases the regulator output voltage).

Figure 5-20. Margin and Trim Circuit for the V3 = 2.5-V Rail

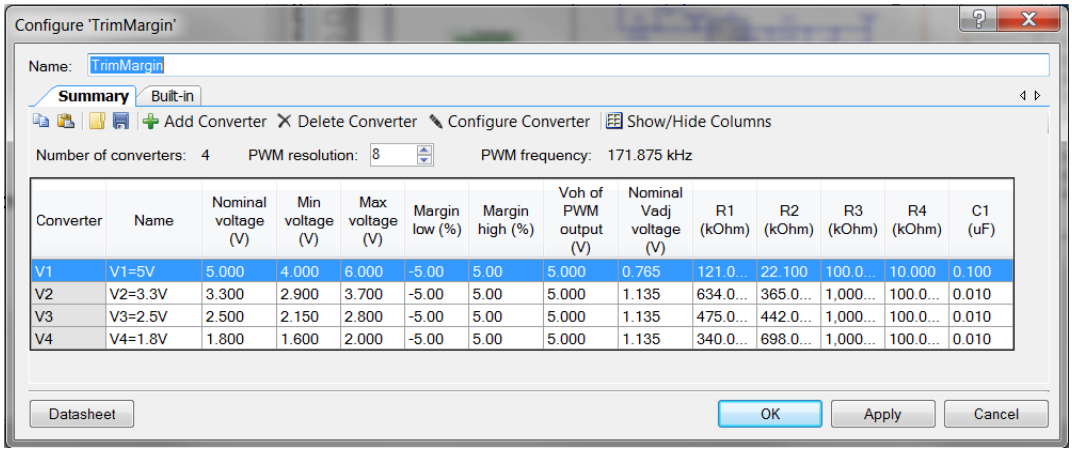


To see the configuration of the **Trim Margin** component, double-click it in the Example 2 top-level design schematic file. This opens the component customizer and the Voltages tab is displayed by default (see Figure 5-21).

For this example project, the key parameter settings are the number of converters, the trim/margin range minimum voltage, and trim/margin range maximum voltage. These together specify the maximum desired pull range from nominal output voltage for either trimming or margining.

Click the **Hardware** tab to configure the PWMs and external hardware components for this example.

Figure 5-21. Trim Margin Voltages Tab

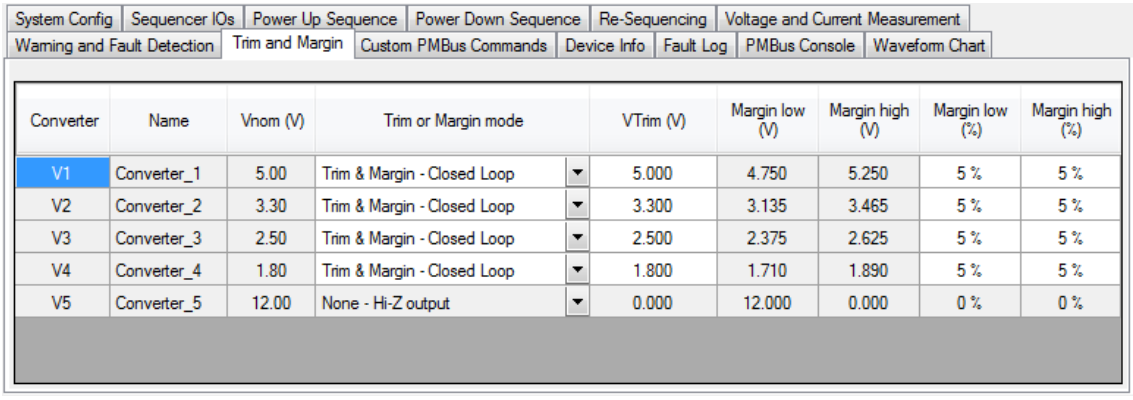


For this example project, the key parameter settings that are PSoC related are PWM resolution and Voh of PWM output (specifies the output high voltage level of the trim/margin outputs). The nominal Vadj voltage, R1, and R2 parameters together describe the external regulator circuit; the values required will be available in the regulator manufacturer's datasheet. The Trim Margin component calculates optimal component values for R3, R4, and C1; you can also enter your own values for these components. These settings have been selected to match the Power Supervision EBK.

Note that from Figure 5-20, R1 = R46, R2 = R51, R3 = R50, R4 = R54, C1 = C15.

Margining is similar to trimming, but is used for a different purpose. In that case, the rails are intentionally set to their upper or lower limits to enable system designers to verify that their systems work at both extremes of the voltage rail tolerances. For example, if a 5-V rail is used in the system and specified to have an accuracy of ±5 percent, margining will set the rail to 5 V –5 percent to enable system verification. Then, the rail can be margined to the high side of 5 V +5 percent and the system verified again. This capability is provided by the Trim Margin component, by calling the MarginLow and MarginHigh APIs. To change the trim/margining settings, click the **Trim and Margin** tab of the Power Supervision Tool.

Figure 5-22. PSoC Power Supervision tool - Trim Margin Tab



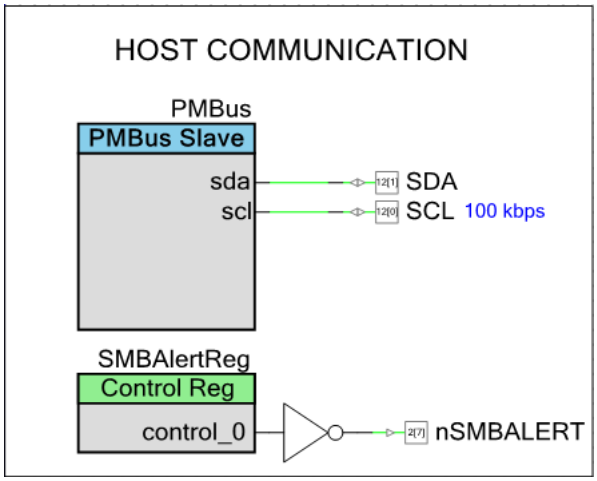
Notice that the default voltage settings have been chosen to be between the OV/UV fault thresholds in the **Warning and Fault Detection** tab. To force an OV and UV fault, set the Margin Low and Margin High values to be 10 percent. Then, press the **Write Changes** button. Read the next section to learn how to set the margins to high and low.

5.2.5 Technical Details - PMBus Interface

The PMBus interface is used as the host interface and configured to support most of the features available in the Power Supervision Tool. Cypress has defined some PMBus manufacturer-specific commands. To see the full list of PMBus protocol and commands supported by this example project, see the PMBus Guide, which is located at `<Install_Directory>\Cypress\PSoC Power Supervision Tool\Documentation`.

The PMBus interface in the example project is configured to run at 100 kpbs and does not support packet error checking (PEC).

Figure 5-23. PMBus Component

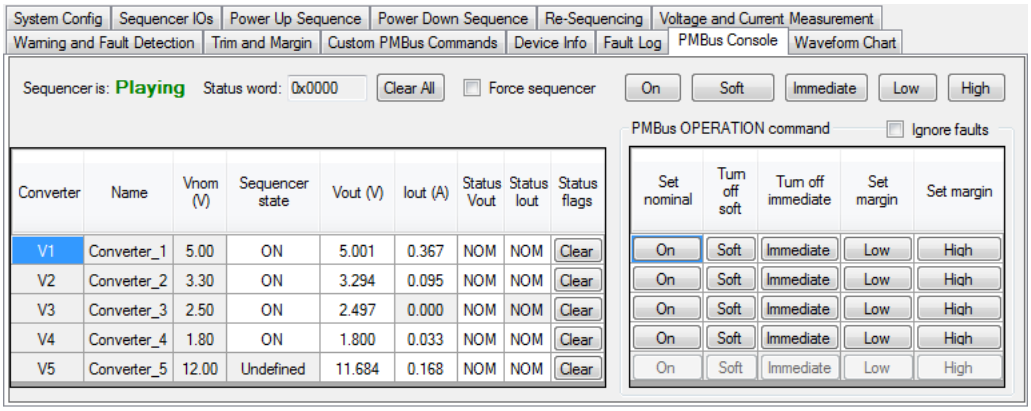


The nSMBALERT pin enables the PSoC to alert the PMBus host that a fault condition had occurred.

All interactions with this example project will be through PMBus commands. Many of the parameters in the PSoC Power Supervision Tool are defined by the PMBus specification. The PSoC Power Supervision Tool incorporates "Tooltips" to help you relate each parameter to the associated PMBus command. Tooltips will pop up when you hover your cursor over a parameter name.

In the PSoC Power Supervision Tool, go to the **PMBus Console** tab to see the ADC post-processed voltage (Vout) and current (Iout) measurements. The Status Vout and Status Iout parameters indicate the standard STATUS_VOUT and STATUS_IOUT PMBus command codes for each of the rails, which are shown in Figure 5-24. Click the **Start Monitor** button to begin reading voltages and currents over PMBus in real time.

Figure 5-24. Power Supervision Tool - PMBus Console



In the same tab, you can turn ON/OFF the rails and set margin HIGH/LOW. The following list shows the behavior of each button:

- **On:** This button turns ON all rails with their respective nominal voltages on the device
- **Soft:** This button turns OFF all rails on the device with user defined *TOFF Delay* values and pgood[x] off prerequisites
- **Immediate:** This button turns OFF all rails on the device immediately after satisfying the pgood[x] off prerequisites
- **Low:** This button sets all rails to their respective *Margin Low (V)* values
- **High:** This button sets all rails to their respective *Margin High (V)* values

The buttons in the table on the right are also used to control single rails with the same description listed above.

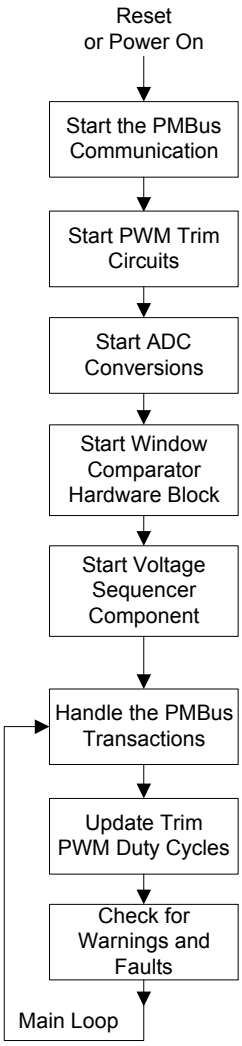
Note that when powering off the 5-V rail, a UV fault may be observed in the 1.8-V, 2.5-V, or 3.3-V rail; this is because the 5-V rail drives the power to these rails. Also, increasing the Margin High or Margin Low thresholds to 10 percent may not cause an OV or UV fault in the configured rail when margining high or low.

5.2.6 Technical Details - Firmware Flowchart

The vast majority of the firmware required for each functional block of the power supervision solution is handled automatically by the provided component APIs and buried interrupt service routines. The only user firmware required for Example 2 is shown in Figure 5-25. The flow is summarized as follows:

1. Initialize hardware components
2. Periodically handle any pending PMBus transaction
3. Periodically check for warnings and faults
4. Periodically running the trim update (active trim) algorithm

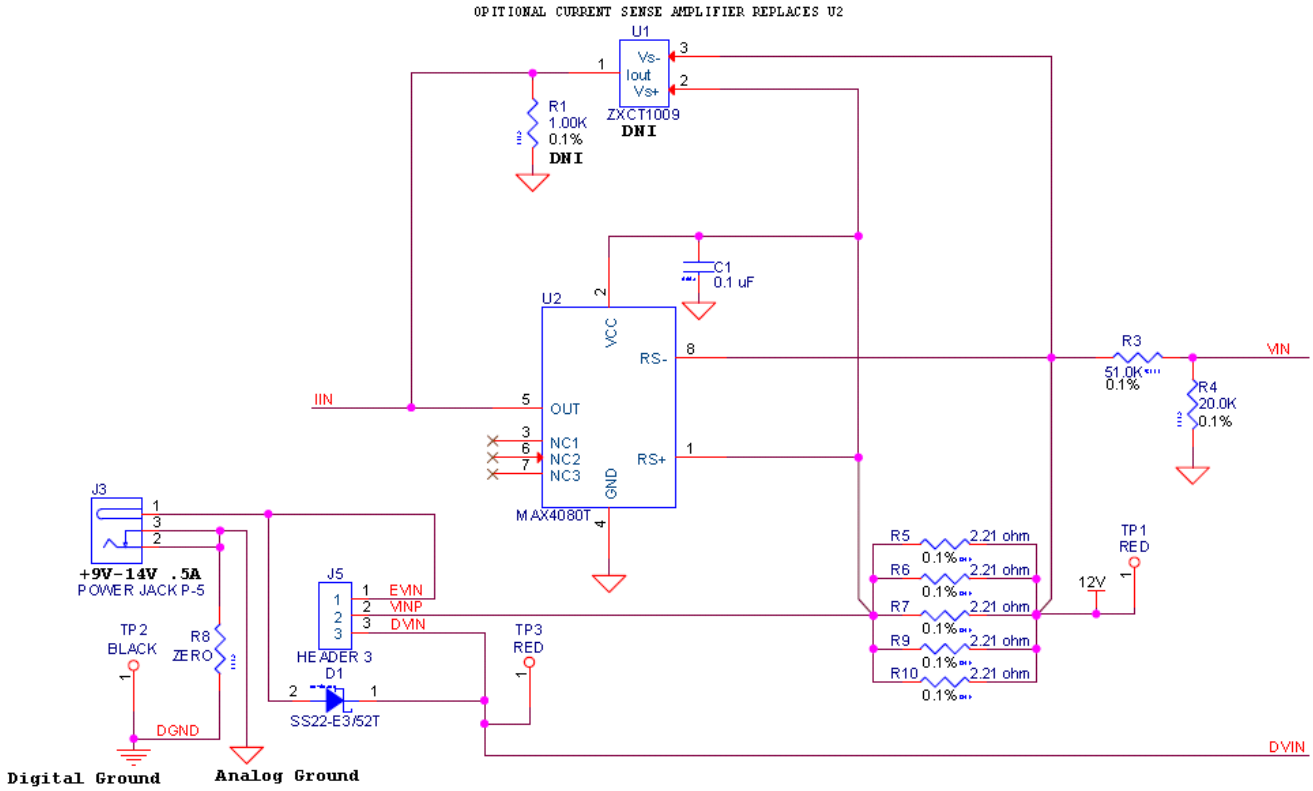
Figure 5-25. Example 2 Firmware Main Loop Flowchart



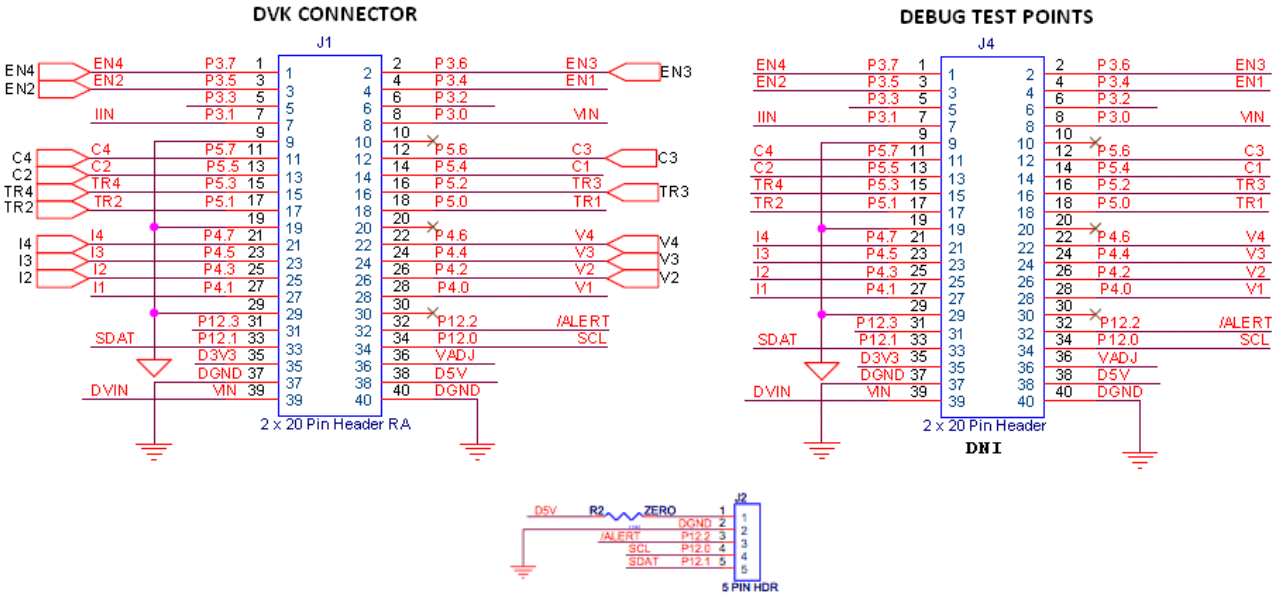
A. Appendix

A.1 Schematic

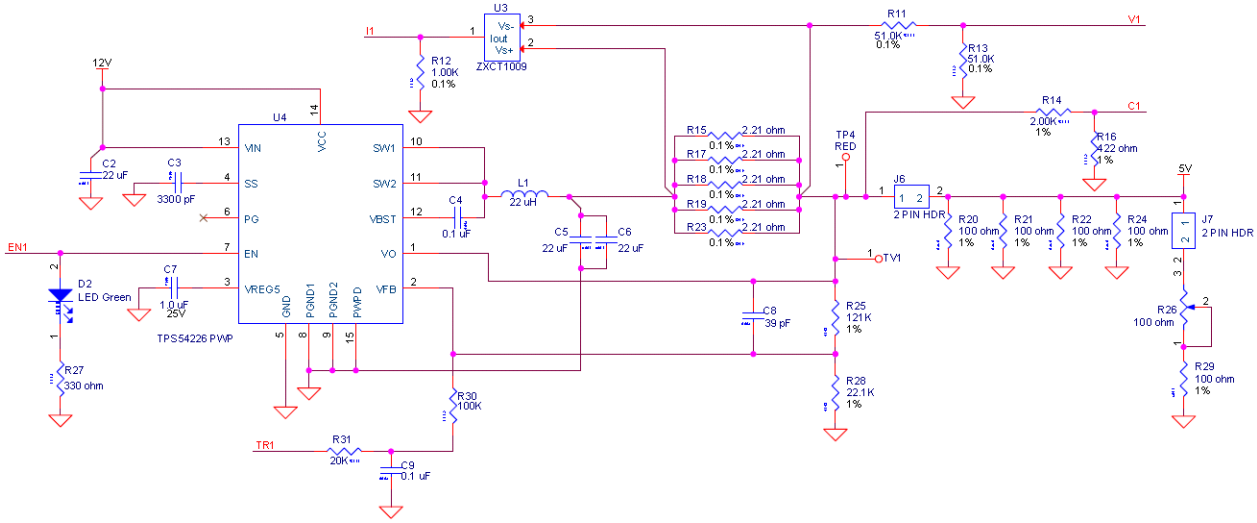
A.1.1 Primary 12-V Power Input



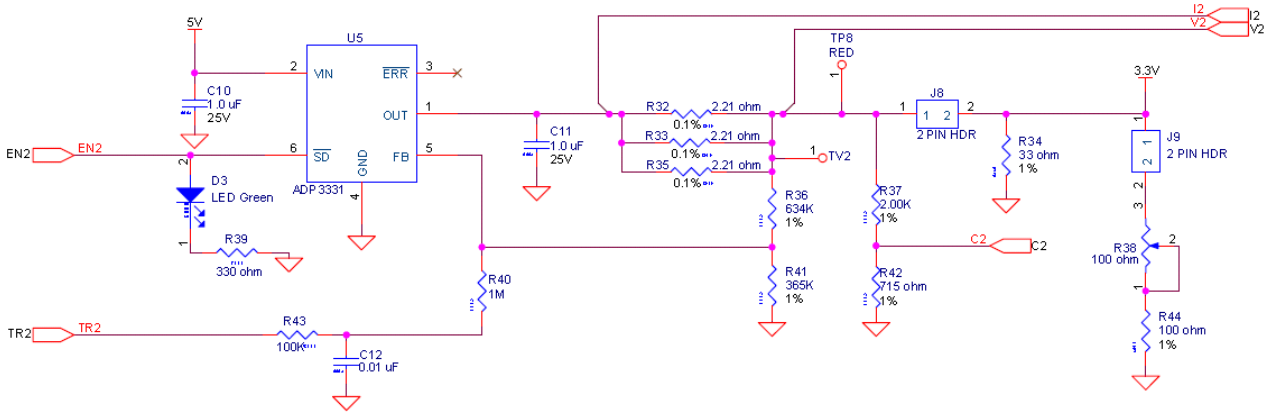
A.1.2 DVK Connector and Debug Test Points



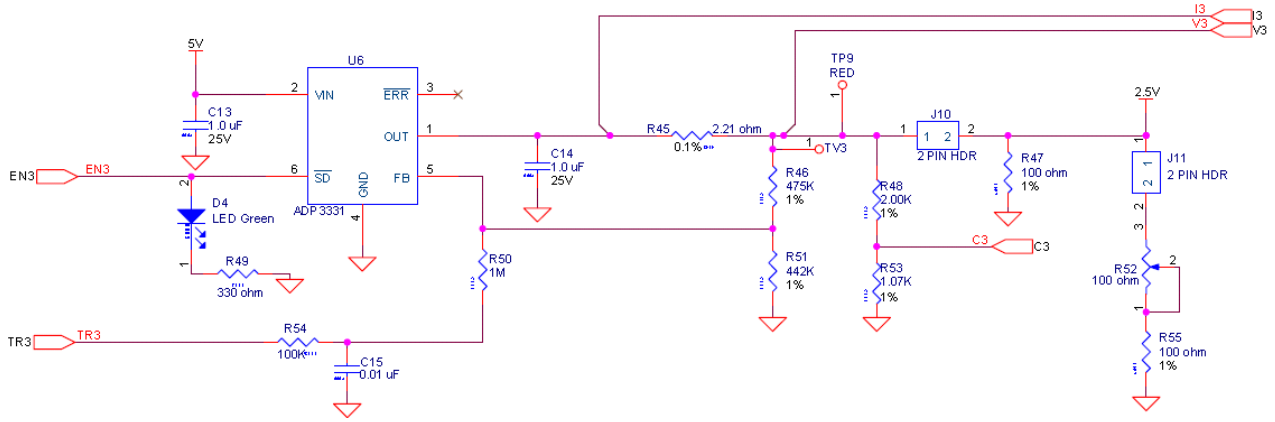
A.1.3 Voltage Regulator V1 = 5 V



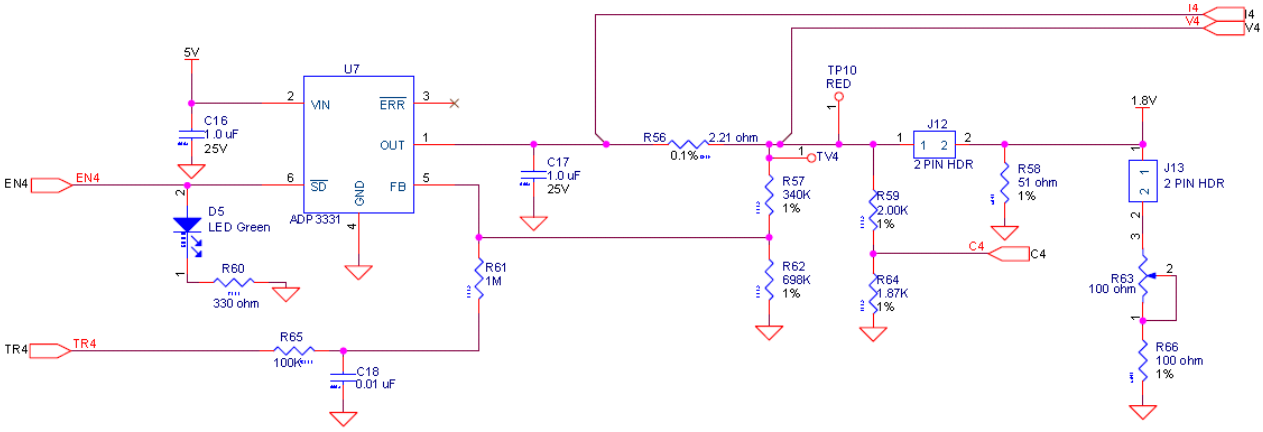
A.1.4 Voltage Regulator V2 = 3.3 V



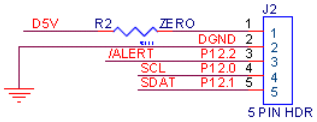
A.1.5 Voltage Regulator V3 = 2.5 V



A.1.6 Voltage Regulator V4 = 1.8 V

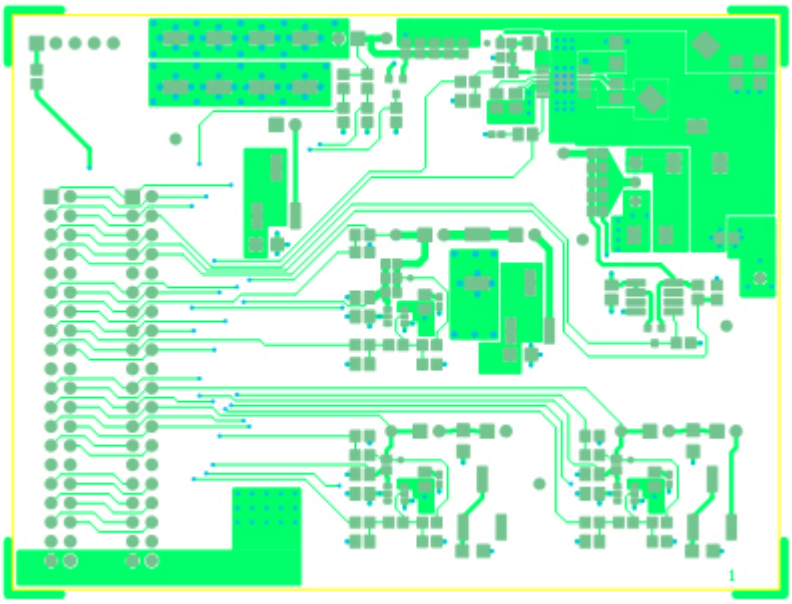


A.1.7 I2C/SMBus/PMBus Interface Connector

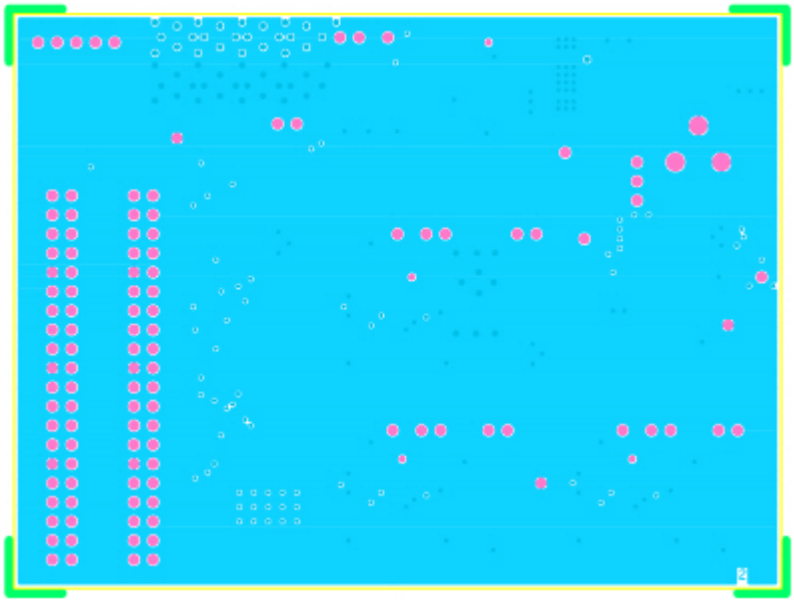


A.2 Layout

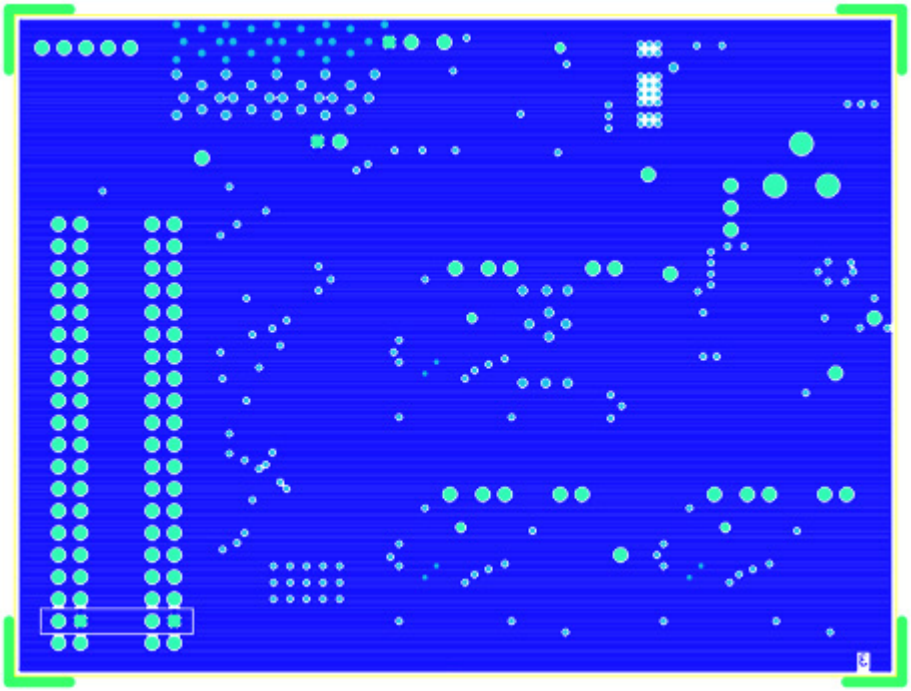
A.2.1 Top Layer



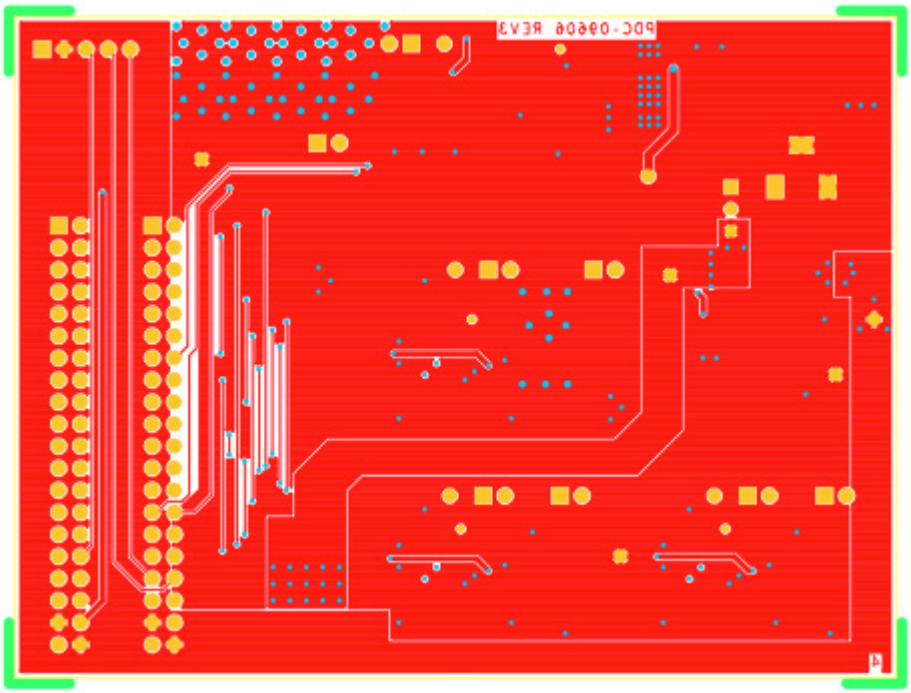
A.2.2 Ground Layer



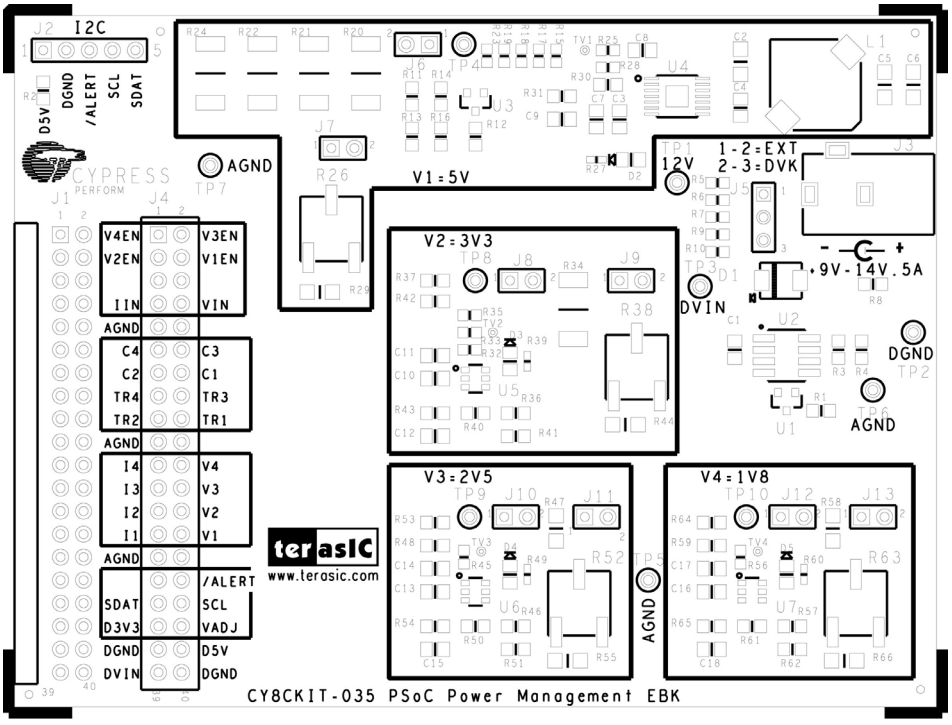
A.2.3 Power Layer



A.2.4 Bottom Layer



A.2.5 Top Silkscreen



A.3 Bill of Materials

Item	Qty.	Value	Description	Designator	Manufacturer	Manufacturer Part#
1	3	0.1µF, 25V	CAP 0.1UF 25V CERAMIC X7R 0805	C1,C4,C9	Kemet	C0805C104K3RAC7210
2	3	22µF, 25V	CAP CER 22UF 25V X5R 1206	C2,C5,C6	Murata Electronics North America	GRM31CR61E226KE15L
3	1	3.3nF, 50V	CAP CER 3300PF 50V 5% C0G 0805	C3	Murata Electronics North America	GRM2165C1H332JA01D
4	7	1.0µF, 25V	CAP CER 1.0UF 25V 10% X5R 0805	C7,C10,C11,C13 C14,C16,C17	Murata Electronics North America	GRM216R61E105KA12D
5	1	39pF, 50V	CAP CERM 39PF 5% 50V NP0 0805	C8	AVX Corporation	08055A390JAT2A
6	3	10nF, 50V	CAP CER 10000PF 50V 10% X7R 0805	C12,C15,C18	Murata Electronics North America	GRM216R71H103KA01D
7	1		DIODE SCHOTTKY 2A 20V SMB	D1	Vishay/General Semiconductor	SS22-E3/52T
8	4		LED GREEN CLEAR 0805 SMD	D2,D3,D4,D5	LITE-ON	LTST-C170GKT
9	1		CONN HEADER R/A DUAL 40POS GOLD	J1	3M	961240-5604-AR
10	1		CONN HEADER 5POS .100 VERT TIN	J2	Molex Inc	22-23-2051
11	1		CONN JACK POWER 2.1mm PCB RA	J3	CUI	PJ-102A
12	1		BERGSTIK II .100" SR STRAIGHT	J5	FCI	68000-403HLF
13	8		CONN HEADER 2 POS .100 VERT TIN	J6,J7,J8,J9,J10, J11,J12,J13	Molex/Waldcom Electronics Corp	22-28-4020
14	1	22µH, 2.2A	COIL PWR CHOKE 22UH 2.2A SMD	L1	Panasonic - ECG	ELL-ATV220M
15	2		RES 0.0 OHM 1/10W 5% 0805 SMD	R2,R8	Panasonic-ECG	ERJ-6GEY0R00V
16	3	51kΩ	RES 51.0K OHM 1/8W 0.1% 0805 SMD	R3,R11,R13	Susumu	RG2012P-513-B-T5
17	1	22kΩ	RES 20.0K OHM 1/8W 0.1% 0805 SMD	R4	Susumu	RG2012P-203-B-T5
18	15	2.21Ω	RES 2.21 OHM 1/16W 0.1% 0603 SMD	R5,R6,R7,R9, R10,R15,R17, R18,R19,R23, R32,R33, R35,R45,R56	Stackpole Electronics Inc	RNCF0603BKC2R21
19	1	1kΩ	RES 1/10W 1K OHM 0.1% 0805	R12	Susumu	RG2012P-102-B-T5
20	4	2kΩ	RES 2.00K OHM 1/8W 1% 0805 SMD	R14,R37,R48, R59	Panasonic - ECG	ERJ-6ENF2001V
21	1	422Ω	RES 422 OHM 1/8W 1% 0805 SMD	R16	Panasonic - ECG	ERJ-6ENF4220V
22	4	100Ω	RES 100 OHM 2W 1% 2512 SMD	R20,R21,R22, R24	Stackpole Electronics Inc	RHC2512FT100R
23	1	121kΩ	RES 121K OHM 1/10W 1% 0603 SMD	R25	Yageo	RC0603FR-07121KL
24	4	100Ω	TRIMPOT 100 OHM 6MM SQ SMD	R26,R38,R52, R63	Bourns Inc.	3361P-1-101GLF
25	4	330Ω	RES 330 OHM 1/16W 5% 0402 SMD	R27,R39,R49, R60	Yageo Corporation	RC0402JR-07330RL
26	1	22.1kΩ	RES 22.1K OHM 1/10W 1% 0603 SMD	R28	Yageo	RC0603FR-0722K1L
27	5	100Ω	RES 100 OHM .5W 1% 1206 SMD	R29,R44,R47, R55,R66	Vishay/Dale	CRCW1206100RFKEAHP

Item	Qty.	Value	Description	Designator	Manufacturer	Manufacturer Part#
28	4	100kΩ	RES 100K OHM 1/8W 5% 0805 SMD	R30,R43,R54, R65	Panasonic - ECG	ERJ-6GEYJ104V
29	1	20kΩ	RES 20K OHM 1/8W 5% 0805 SMD	R31	Panasonic - ECG	ERJ-6GEYJ203V
30	1	33Ω	RES 33 OHM 2W 1% 2512 SMD	R34	Stackpole Electronics Inc	RHC2512FT33R0
31	1	634kΩ	RES 634K OHM 1/8W 1% 0805 SMD	R36	Panasonic - ECG	ERJ-6ENF6343V
32	3	1MΩ	RES 1M OHM 1/10W 5% 0805 SMD	R40,R50,R61	Panasonic - ECG	ERJ-6GEYJ105V
33	1	365kΩ	RES 365K OHM 1/8W 1% 0805 SMD	R41	Panasonic - ECG	ERJ-6ENF3653V
34	1	715Ω	RES 715 OHM 1/8W 1% 0805 SMD	R42	Panasonic - ECG	ERJ-6ENF7150V
35	1	475kΩ	RES 475K OHM 1/8W 1% 0805 SMD	R46	Panasonic - ECG	ERJ-6ENF4753V
36	1	442kΩ	RES 442K OHM 1/8W 1% 0805 SMD	R51	Panasonic - ECG	ERJ-6ENF4423V
37	1	1.07kΩ	RES 1.07K OHM 1/8W 1% 0805 SMD	R53	Panasonic - ECG	ERJ-6ENF1071V
38	1	340kΩ	RES 340K OHM 1/8W 1% 0805 SMD	R57	Panasonic - ECG	ERJ-6ENF3403V
39	1	51Ω	RES 51.0 OHM 1/4W 1% 1206 SMD	R58	Vishay/Dale	CRCW120651R0FKEA
40	1	698kΩ	RES 698K OHM 1/8W 1% 0805 SMD	R62	Panasonic - ECG	ERJ-6ENF6983V
41	1	1.87kΩ	RES 1.87K OHM 1/8W 1% 0805 SMD	R64	Panasonic - ECG	ERJ-6ENF1871V
42	6		TEST POINT 43 HOLE 65 PLATED RED	TP1,TP3,TP4, TP8,TP9,TP10	Keystone Electronics	5000
43	4		TEST POINT 43 HOLE 65 PLATED BLACK	TP2,TP5,TP6, TP7	Keystone Electronics	5001
44	1		IC AMP CURRENT SENSE 8-SOIC	U2	Maxim Integrated Prod-ucts	MAX4080TASA+
45	1		HIGH-SIDE CURRENT MONITOR	U3	Zetex	ZXCT1009FTA
46	1		IC CONV STP-DWN SYNC 2A 14HTSSOP	U4	Texas Instruments	TPS54226PWPR
47	3		IC REG LDO ADJ 200MA SOT-23-6	U5,U6,U7	Analog Devices Inc	ADP3331ARTZ-REEL7
48	4		BUMPER WHITE .500X.23 SQUARE	See Assembly Drawing	Richco Plastics Co.	RBS-3R
49	9		SHUNT GOLD W/HANDLE, BLACK		Kobiconn	151-8030-E
No Load Components						
50	1	1kΩ	RES 1K 1/10W OHM 0.1% 0805	R1	Stackpole Electronics Inc	RNCF0805BTC1K00
51	1		CONN HEADER VERT DUAL 40POS GOLD	J4	3M	961240-6404-AR
52	1		HIGH-SIDE CURRENT MONITOR	U1	Zetex	ZXCT1009FTA
53	4		TEST VIA 40 HOLE 20 PLATED	TV1,TV2,TV3, TV4	NONE	NA

Revision History

CY8CKIT-035 PSoC® 3 and PSoC 5LP Power Supervision Expansion Board Kit (EBK) Guide Revision History

Document Title: CY8CKIT-035 PSoC® 3 and PSoC 5LP Power Supervision Expansion Board Kit (EBK) Guide Document Number: 001-86225				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	4556148	05/22/2015	RLOS	Initial version of the kit guide
*A	4952129	10/07/2015	RLOS	Updated Software Installation chapter on page 8: Updated "Install Software" on page 9: Updated description. Updated Example Projects chapter on page 27: Updated "Example Project 1: Advanced Sequencer" on page 27: Updated "Technical Details - UV/OV Monitoring using the Window Comparator" on page 32: Updated description. Updated Figure 5-8. Updated Figure 5-9. Updated Figure 5-10. Updated "Example Project 2: Power Supervision" on page 35: Updated "Technical Details - Regulator Trimming and Margining" on page 42: Updated Figure 5-21. Removed figure "Trim Margin Hardware Tab". Updated description.
*B	5025927	11/24/2015	GRSK	Updated Software Installation chapter on page 8: Updated "Install Software" on page 9: Updated description.