TREX-S2-TMB

Motherboard for Stratix II FPGA Module

Data Book

TREX-S2-TMB

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Chapter 1

Introduction

TREX-S2-TMB is a motherboard developed exclusively for **TREX-S2** module which enables users to use ALL the powerful features of Altera StratixII FPGAs without having to worry about how to design the complex circuitry for power supply and configuration. Also, **TREX-S2-TMB** users can access various memory devices (SRAM, SDRAM, DDRII SDRAM) without having to worry about how to create and manufacture the complex motherboard.

Users should read the **TREX-S2** Data Book before reading this manual.

Features

Figure 1.1 shows the photo of the **TREX-S2-TMB** motherboard. Figure 1.2 shows the photo **TREX-S2** FPGA module plugged on the **TREX-S2-TMB** motherboard. The important features are listed below:

- ✓ For TREX-S2 FPGA Module
- ✓ Provide three 70-pin 2.54mm-pitch connectors to allow users to directly access about 210 pins of the TREX-S2 FPGA module; adjustable **VCCB to 3.3V or 1.8V to set VCCIO in this bank group.**
- ✓ Provide four 40-pin IDE connectors; voltage is fixed to 3.3v.
- ✓ Provide SRAM with 256K(up to 512K) x 16bits x 2banks
- ✓ Provide SDRAM with 16M x 32bits
- ✓ Provide DDRII SRAM with 16M(up to 64M) x 16bits x 2banks
- ✓ Provide three clock sources (50Mhz, 27Mhz and EXTCLK socket for external clock)
- ✓ Two independent programming circuits (JTAG and AS Mode)
- ✓ 8 User LEDs
- ✓ 1 Push Button
- ✓ Provide 5V cooling fun power
- ✓ Provide RS232 port

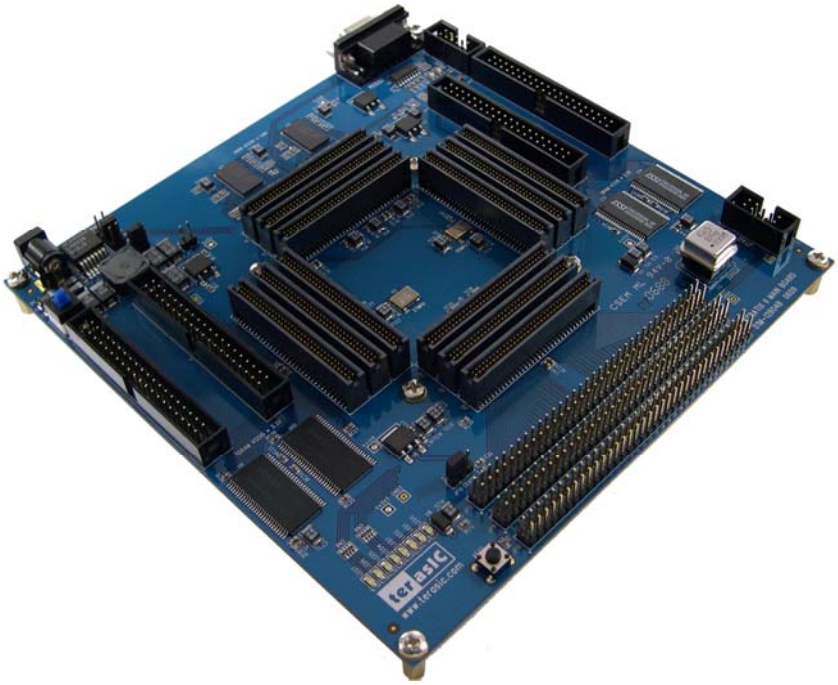


Figure 1.1. The TREX-S2-TMB Motherboard

Figure 1.2. TREX-S2 FPGA module plugged onto the TREX-S2-TMB motherboard

TREX-S2 Motherboard Selection Guide

TREX-S2 module has a series of motherboards designed for various applications. The available product portfolio is listed below. To request the detailed specification of the TREX-S2 motherboard, please send email to support@terasic.com. Figure 1.4 shows the TREX-S2 module with **TREX-S2-TMB** motherboard.

Product Code	Applications	Listing Price	Spec File Name
TREX-S2-TMA	**Prototyping**	**$325**	**TREXS2_TMA.pdf**
TREX-S2-TMB	**Prototyping with DDRII, SRAM, SDRAM**	**$395**	**TREXS2_TMB.pdf**

Figure 1.3 Terasic TREX-S2 Motherboard Part Number

Figure 1.4 Terasic TREX-S2 Module with TREX-S2-TMA Motherboard

Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000
- ✓ English Support Line: +1-403-512-1336

Chapter 2

Architecture

This chapter describes the architecture of the **TREX-S2-TMB** motherboard including block diagram, connectors, and clocking system.

The Block Diagram

The block diagram of the **TREX-S2-TMB** module is described in Figure 2.1.

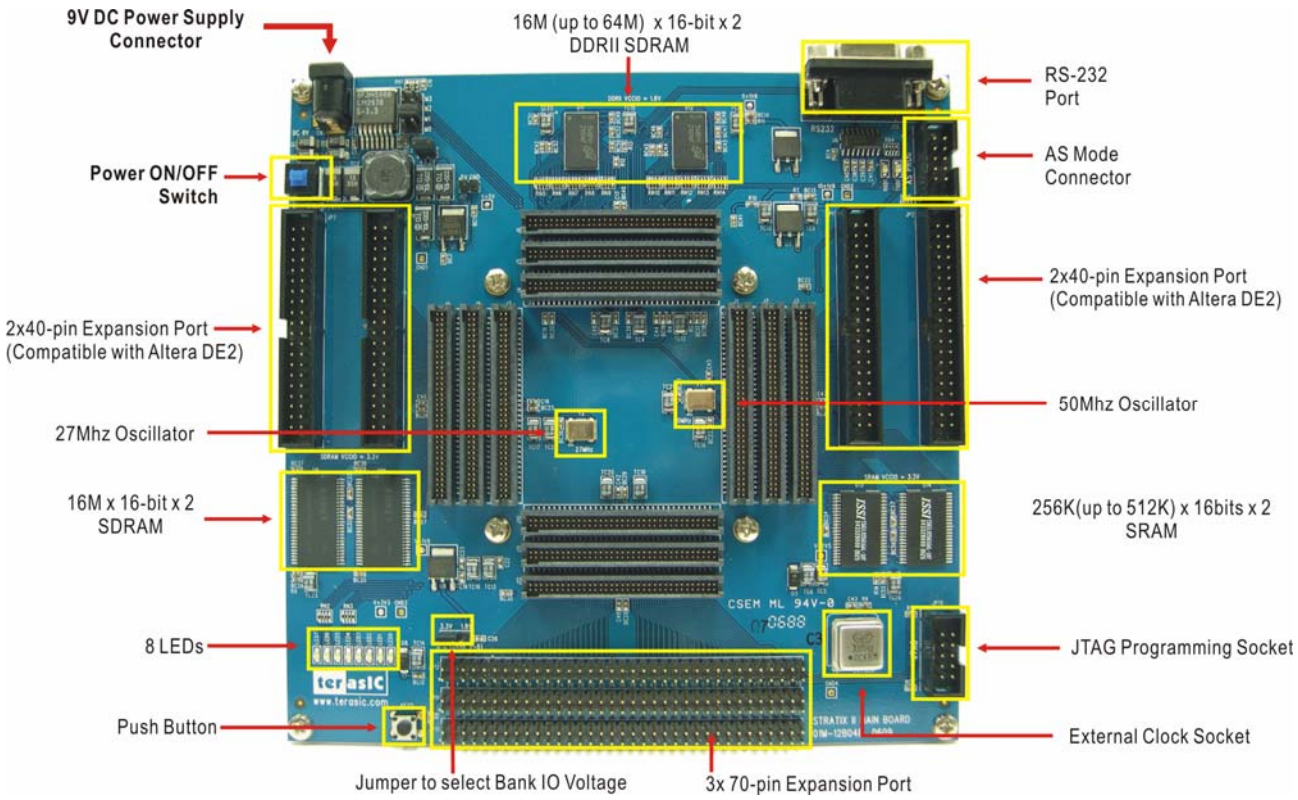


Figure 2.1 Terasic TREX-S2-TMB Module Block Diagram

Connectors

Figure 2.2 shows the connector and component diagram of the TREX-S2-TMB motherboard. Note that each pin in **JPN** connector is connected to the same pin in the **JN** connector of the **TREX-S2** module, where N = 10~12.

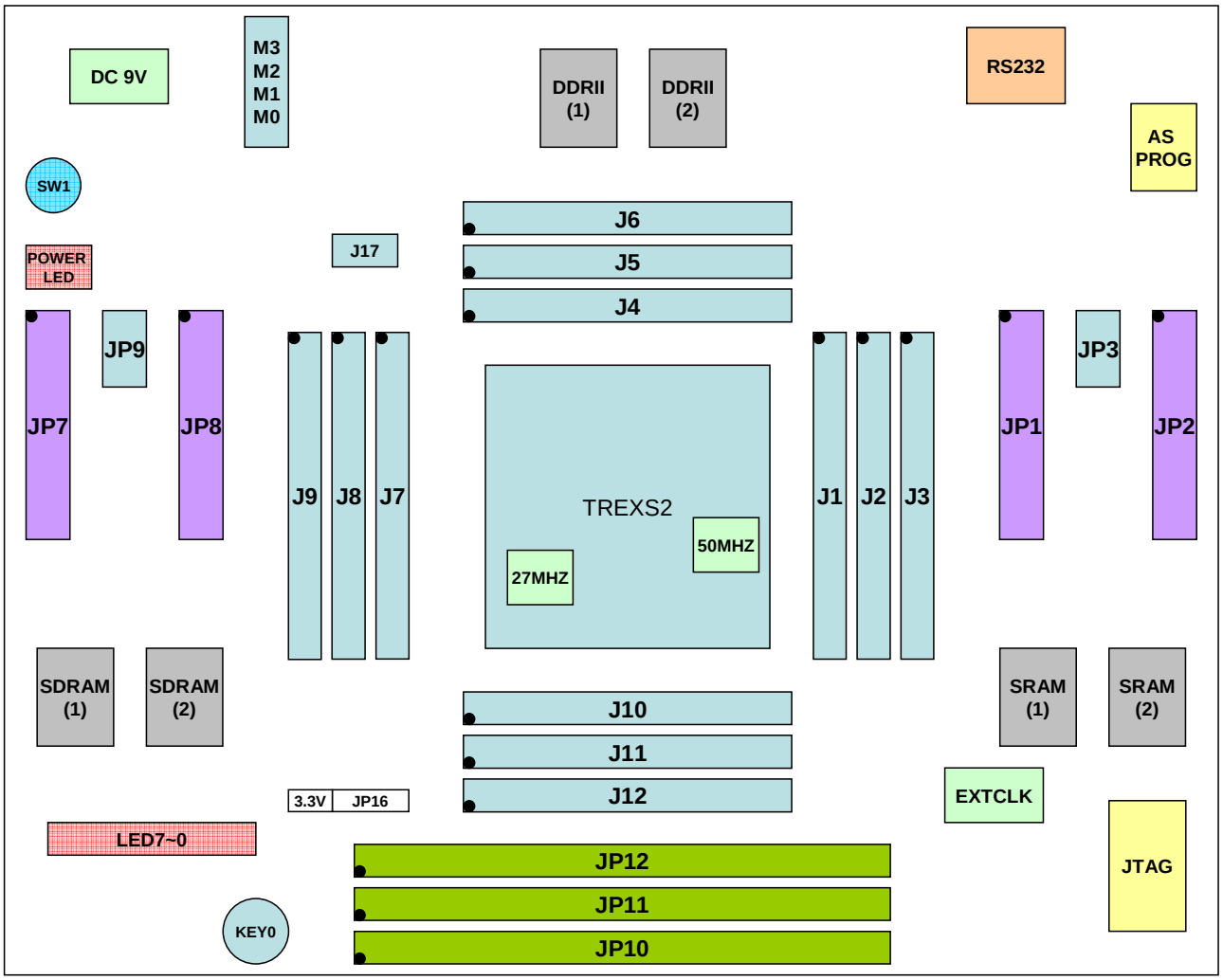


Figure 2.2. TREX-S2-TMB Motherboard Connector

Important Pin Assignment

Power ON/OFF and Power Indicator

- ✓ Power Jack (DC 9V) is for 9V DC Input
- ✓ Power Switch (SW1) is for power ON/OFF control.
- ✓ Power LED (POWER1) is for indicating the power status.

Cooling fun power connector

✓ J17 is used to provide the 5V power for cooling fan.

Pin	Voltage
1	5V
2	GND

Clocking Source

Name	StratixII Pin
50MHz	T30, U32
27MHz	U1, U3, AJ3
EXTCLK	T32, AJ30

Configuration Mode

✓ Support JTAG and AS Mode

✓ All the signals for JTAG and AS Mode are also shown in the surrounding connectors (J1-J12)

JTAG Mode

Name	StratixII Pin	Schematic Name	Connector
TCK	AF24	TRGTCK	J12(59)
TMS	AE24	TRGTMS	J12(60)
TDI	AL31	TRGTDI	J12(67)
TDO	C3	TRGTDO	J5(4)
TRST	AK30	TRGRESET	J12(68)

AS Mode

Name	StratixII Pin	Schematic Name	Connector
DCLK	B31	TRGDCLK	J6(68)
NCE	C30	TRGNCE	J6(67)
NCSO	G19	TRGNCSO	J5(43)
ASDO	F17	TRGASDO	J5(39)
DATA0	H19	TRGDATA0	J6(44)

User LEDs (LED 7 – 0)

✓ User can drive **0** to the corresponding pin to turn ON the LED.

Name	StratixII Pin
LED0	AF2
LED1	AF1
LED2	AG2
LED3	AG1
LED4	AH2
LED5	AH1
LED6	AJ2
LED7	AJ1

Pushbutton – KEY0

✓ The pushbutton is an active-low device – logic level 0 is obtained when the KEY is pressed.

Name	StratixII Pin
KEY0	AK4

RS-232 Port

✓ The RS232 circuit is built on the motherboard to provide users a tool to communicate with the user logic in FPGA.

Name	StratixII Pin
TXD	E30
RXD	E29

40 PIN GPIO Header

✓ JP1, JP2, JP7 and JP8 are four 40-pin GPIO connectors; voltage is fixed to 3.3v

.

We used different colors to annotate each pin in each connector. The color annotation table is listed below.

RED	Power 3.3V	PINK	Power 5V
GREEN	Power GND	YELLOW	Dedicated Clock
WHITE	GPIO		

JP1					
PIN	PinOut	Function	PI	PinOut	Function
1	H27	GPIO_0	2	H28	GPIO_1
3	J26	GPIO_2	4	J27	GPIO_3
5	K24	GPIO_4	6	K25	GPIO_5
7	K29	GPIO_6	8	K30	GPIO_7
9	F29	GPIO_8	10	F30	GPIO_9
11	IOVCC5	VCC 5V	12	GND	GND
13	G29	GPIO_10	14	G30	GPIO_11
15	H29	GPIO_12	16	H30	GPIO_13
17	K26	GPIO_14	18	K27	GPIO_15
19	L23	GPIO_16	20	L24	GPIO_17
21	L29	GPIO_18	22	L30	GPIO_19
23	M24	GPIO_20	24	M25	GPIO_21
25	M29	GPIO_22	26	M30	GPIO_23
27	N26	GPIO_24	28	N27	GPIO_25
29	IOVCC3	VCC 3.3V	31	GND	GND
31	N30	GPIO_26	32	N31	GPIO_27
33	P26	GPIO_28	34	P27	GPIO_29
35	R24	GPIO_30	36	R25	GPIO_31
37	R28	GPIO_32	38	R29 D30	GPIO_33 DCLK
39	T27	GPIO_34	40	T28	GPIO_35

JP2					
PIN	PinOut	Function	PI	PinOut	Function
1	D31	GPIO_0	2	D32	GPIO_1
3	E31	GPIO_2	4	E32	GPIO_3
5	F31	GPIO_4	6	F32	GPIO_5
7	G31	GPIO_6	8	G32	GPIO_7
9	H31	GPIO_8	10	H32	GPIO_9
11	IOVCC5	VCC 5V	12	GND	GND
13	J31	GPIO_10	14	J32	GPIO_11
15	K31	GPIO_12	16	K32	GPIO_13
17	L31	GPIO_14	18	L32	GPIO_15
19	M31	GPIO_16	20	M32	GPIO_17
21	P31	GPIO_18	22	P32	GPIO_19
23	R30	GPIO_20	24	R31	GPIO_21
25	M26	GPIO_22	26	M27	GPIO_23
27	N24	GPIO_24	28	N25	GPIO_25
29	IOVCC3	VCC 3.3V	31	GND	GND
31	N28	GPIO_26	32	N29	GPIO_27
33	P24	GPIO_28	34	P25	GPIO_29
35	P28	GPIO_30	36	P29	GPIO_31
37	R26	GPIO_32	38	R27 U30	GPIO_33 DCLK
39	T22	GPIO_34	40	T23	GPIO_35

JP7					
PI	PinOut	Function	PI	PinOut	Function
1	D1	GPIO_0	2	D2	GPIO_1
3	E1	GPIO_2	4	E2	GPIO_3
5	F1	GPIO_4	6	F2	GPIO_5
7	G1	GPIO_6	8	G2	GPIO_7
9	H1	GPIO_8	10	H2	GPIO_9
11	IOVCC5	VCC 5V	12	GND	GND
13	J1	GPIO_10	14	J2	GPIO_11
15	K1	GPIO_12	16	K2	GPIO_13
17	L1	GPIO_14	18	L2	GPIO_15
19	M1	GPIO_16	20	M2	GPIO_17
21	P1	GPIO_18	22	P2	GPIO_19
23	R2	GPIO_20	24	R3	GPIO_21
25	M6	GPIO_22	26	M7	GPIO_23
27	N2	GPIO_24	28	N3	GPIO_25
29	IOVCC3	VCC 3.3V	31	GND	GND
31	N6	GPIO_26	32	N7	GPIO_27
33	P4	GPIO_28	34	P5	GPIO_29
35	P8	GPIO_30	36	P9	GPIO_31
37	R6	GPIO_32	38	R7 T3	GPIO_33 **DCLK**
39	T5	GPIO_34	40	T6	GPIO_35

JP8					
PIN	PinOut	Function	PI	PinOut	Function
1	E3	GPIO_0	2	E4	GPIO_1
3	G3	GPIO_2	4	G4	GPIO_3
5	J6	GPIO_4	6	J7	GPIO_5
7	K3	GPIO_6	8	K4	GPIO_7
9	F3	GPIO_8	10	F4	GPIO_9
11	IOVCC5	VCC 5V	12	GND	GND
13	J3	GPIO_10	14	J4	GPIO_11
15	J8	GPIO_12	16	J9	GPIO_13
17	K6	GPIO_14	18	K7	GPIO_15
19	L3	GPIO_16	20	L4	GPIO_17
21	L7	GPIO_18	22	L8	GPIO_19
23	M3	GPIO_20	24	M4	GPIO_21
25	M8	GPIO_22	26	M9	GPIO_23
27	N4	GPIO_24	28	N5	GPIO_25
29	IOVCC3	VCC 3.3V	31	GND	GND
31	N8	GPIO_26	32	N9	GPIO_27
33	P6	GPIO_28	34	P7	GPIO_29
35	R4	GPIO_30	36	R5	GPIO_31
37	R10	GPIO_32	38	R11 D3	GPIO_33 DCLK
39	T10	GPIO_34	40	T11	GPIO_35

SRAM

✓ Two independent SRAM bank, maximum size up to 512K * 16bits for each bank.

SRAM 1		
Name	PinOut	Description
SRAM_1ADDR[0]	PIN_V30	SRAM Address 0
SRAM_1ADDR[1]	PIN_W31	SRAM Address 1
SRAM_1ADDR[2]	PIN_AA31	SRAM Address 2
SRAM_1ADDR[3]	PIN_AB31	SRAM Address 3
SRAM_1ADDR[4]	PIN_AC31	SRAM Address 4
SRAM_1ADDR[5]	PIN_AE31	SRAM Address 5
SRAM_1ADDR[6]	PIN_AF31	SRAM Address 6
SRAM_1ADDR[7]	PIN_AG31	SRAM Address 7
SRAM_1ADDR[8]	PIN_AH31	SRAM Address 8
SRAM_1ADDR[9]	PIN_AJ31	SRAM Address 9
SRAM_1ADDR[10]	PIN_AG29	SRAM Address 10
SRAM_1ADDR[11]	PIN_AG30	SRAM Address 11
SRAM_1ADDR[12]	PIN_AE29	SRAM Address 12
SRAM_1ADDR[13]	PIN_AE30	SRAM Address 13
SRAM_1ADDR[14]	PIN_AE25	SRAM Address 14
SRAM_1ADDR[15]	PIN_AC25	SRAM Address 15
SRAM_1ADDR[16]	PIN_AB27	SRAM Address 16
SRAM_1ADDR[17]	PIN_AB28	SRAM Address 17
SRAM_1ADDR[18]	PIN_AE26	SRAM Address 18
SRAM_1BE_N[0]	PIN_AD26	SRAM Byte Enable
SRAM_1BE_N[1]	PIN_AD27	SRAM Byte Enable
SRAM_1DQ[0]	PIN_AH29	SRAM Data 0
SRAM_1DQ[1]	PIN_AH30	SRAM Data 1
SRAM_1DQ[2]	PIN_AF29	SRAM Data 2
SRAM_1DQ[3]	PIN_AF30	SRAM Data 3
SRAM_1DQ[4]	PIN_AE27	SRAM Data 4
SRAM_1DQ[5]	PIN_AE28	SRAM Data 5
SRAM_1DQ[6]	PIN_AD24	SRAM Data 6
SRAM_1DQ[7]	PIN_AD25	SRAM Data 7
SRAM_1DQ[8]	PIN_AC26	SRAM Data 8
SRAM_1DQ[9]	PIN_AC27	SRAM Data 9
SRAM_1DQ[10]	PIN_AB29	SRAM Data 10
SRAM_1DQ[11]	PIN_AB30	SRAM Data 11
SRAM_1DQ[12]	PIN_AB25	SRAM Data 12
SRAM_1DQ[13]	PIN_AB26	SRAM Data 13
SRAM_1DQ[14]	PIN_AA29	SRAM Data 14
SRAM_1DQ[15]	PIN_AA30	SRAM Data 15
SRAM_1OE_N	PIN_AC24	SRAM Output Enable
SRAM_1WE_N	PIN_AD31	SRAM Write Enable

SRAM 2		
Name	PinOut	Description
SRAM_2ADDR[0]	PIN_V31	SRAM Address 0
SRAM_2ADDR[1]	PIN_W32	SRAM Address 1
SRAM_2ADDR[2]	PIN_AA32	SRAM Address 2
SRAM_2ADDR[3]	PIN_AB32	SRAM Address 3
SRAM_2ADDR[4]	PIN_AC32	SRAM Address 4
SRAM_2ADDR[5]	PIN_AE32	SRAM Address 5
SRAM_2ADDR[6]	PIN_AF32	SRAM Address 6
SRAM_2ADDR[7]	PIN_AG32	SRAM Address 7
SRAM_2ADDR[8]	PIN_AH32	SRAM Address 8
SRAM_2ADDR[9]	PIN_AJ32	SRAM Address 9
SRAM_2ADDR[10]	PIN_AB23	SRAM Address 10
SRAM_2ADDR[11]	PIN_AB24	SRAM Address 11
SRAM_2ADDR[12]	PIN_AA26	SRAM Address 12
SRAM_2ADDR[13]	PIN_AA27	SRAM Address 13
SRAM_2ADDR[14]	PIN_Y30	SRAM Address 14
SRAM_2ADDR[15]	PIN_V24	SRAM Address 15
SRAM_2ADDR[16]	PIN_U22	SRAM Address 16
SRAM_2ADDR[17]	PIN_U23	SRAM Address 17
SRAM_2ADDR[18]	PIN_Y31	SRAM Address 18
SRAM_2BE_N[0]	PIN_W24	SRAM Byte Enable
SRAM_2BE_N[1]	PIN_W25	SRAM Byte Enable
SRAM_2DQ[0]	PIN_AA24	SRAM Data 0
SRAM_2DQ[1]	PIN_AA25	SRAM Data 1
SRAM_2DQ[2]	PIN_Y28	SRAM Data 2
SRAM_2DQ[3]	PIN_Y29	SRAM Data 3
SRAM_2DQ[4]	PIN_Y24	SRAM Data 4
SRAM_2DQ[5]	PIN_Y25	SRAM Data 5
SRAM_2DQ[6]	PIN_W26	SRAM Data 6
SRAM_2DQ[7]	PIN_W27	SRAM Data 7
SRAM_2DQ[8]	PIN_V28	SRAM Data 8
SRAM_2DQ[9]	PIN_V29	SRAM Data 9
SRAM_2DQ[10]	PIN_U27	SRAM Data 10
SRAM_2DQ[11]	PIN_U28	SRAM Data 11
SRAM_2DQ[12]	PIN_Y26	SRAM Data 12
SRAM_2DQ[13]	PIN_Y27	SRAM Data 13
SRAM_2DQ[14]	PIN_W28	SRAM Data 14
SRAM_2DQ[15]	PIN_W29	SRAM Data 15
SRAM_2OE_N	PIN_V23	SRAM Output Enable
SRAM_2WE_N	PIN_AD32	SRAM Write Enable

SDRAM

✓ A combinational 32-bit data width SDRAM bank.

SDRAM		
Name	PinOut	Description
DRAM_ADDR[0]	PIN_AB9	SDRAM Address 0
DRAM_ADDR[1]	PIN_AC6	SDRAM Address 1
DRAM_ADDR[2]	PIN_AD8	SDRAM Address 2
DRAM_ADDR[3]	PIN_AD9	SDRAM Address 3
DRAM_ADDR[4]	PIN_AC7	SDRAM Address 4
DRAM_ADDR[5]	PIN_AB10	SDRAM Address 5
DRAM_ADDR[6]	PIN_AB6	SDRAM Address 6
DRAM_ADDR[7]	PIN_AA9	SDRAM Address 7
DRAM_ADDR[8]	PIN_AA4	SDRAM Address 8
DRAM_ADDR[9]	PIN_Y7	SDRAM Address 9
DRAM_ADDR[10]	PIN_AB5	SDRAM Address 10
DRAM_ADDR[11]	PIN_Y3	SDRAM Address 11
DRAM_ADDR[12]	PIN_W7	SDRAM Address 12
DRAM_BA_0	PIN_AA3	SDRAM Bank Address 0
DRAM_BA_1	PIN_AA8	SDRAM Bank Address 1
DRAM_CAS_N	PIN_W6	SDRAM Column Address Strobe
DRAM_CKE	PIN_V10	SDRAM Clock Enable
DRAM_CLK	PIN_AE1	SDRAM Clock
DRAM_CS_N	PIN_Y6	SDRAM Chip Enable
DRAM_DQ[0]	PIN_U10	SDRAM Data 0
DRAM_DQ[1]	PIN_U11	SDRAM Data 1
DRAM_DQ[2]	PIN_V6	SDRAM Data 2
DRAM_DQ[3]	PIN_V7	SDRAM Data 3
DRAM_DQ[4]	PIN_W4	SDRAM Data 4
DRAM_DQ[5]	PIN_W5	SDRAM Data 5
DRAM_DQ[6]	PIN_W8	SDRAM Data 6
DRAM_DQ[7]	PIN_W9	SDRAM Data 7
DRAM_DQ[8]	PIN_Y4	SDRAM Data 8
DRAM_DQ[9]	PIN_Y5	SDRAM Data 9
DRAM_DQ[10]	PIN_Y8	SDRAM Data 10
DRAM_DQ[11]	PIN_Y9	SDRAM Data 11
DRAM_DQ[12]	PIN_AA6	SDRAM Data 12
DRAM_DQ[13]	PIN_AA7	SDRAM Data 13
DRAM_DQ[14]	PIN_AB3	SDRAM Data 14
DRAM_DQ[15]	PIN_AB4	SDRAM Data 15
DRAM_DQ[16]	PIN_AB7	SDRAM Data 16
DRAM_DQ[17]	PIN_AB8	SDRAM Data 17
DRAM_DQ[18]	PIN_AC3	SDRAM Data 18
DRAM_DQ[19]	PIN_AC4	SDRAM Data 19
DRAM_DQ[20]	PIN_AC8	SDRAM Data 20
DRAM_DQ[21]	PIN_AC9	SDRAM Data 21
DRAM_DQ[22]	PIN_AG3	SDRAM Data 22
DRAM_DQ[23]	PIN_AG4	SDRAM Data 23

DRAM_DQ[24]	PIN_AH4	SDRAM Data 24
DRAM_DQ[25]	PIN_AH3	SDRAM Data 25
DRAM_DQ[26]	PIN_AF4	SDRAM Data 26
DRAM_DQ[27]	PIN_AF3	SDRAM Data 27
DRAM_DQ[28]	PIN_AE4	SDRAM Data 28
DRAM_DQ[29]	PIN_AE3	SDRAM Data 29
DRAM_DQ[30]	PIN_AD7	SDRAM Data 30
DRAM_DQ[31]	PIN_AD6	SDRAM Data 31
DRAM_DQM[0]	PIN_U5	SDRAM Data Mask 0
DRAM_DQM[1]	PIN_U6	SDRAM Data Mask 1
DRAM_DQM[2]	PIN_V4	SDRAM Data Mask 2
DRAM_DQM[3]	PIN_V5	SDRAM Data Mask 3
DRAM_RAS_N	PIN_Y2	SDRAM Row Address Strobe
DRAM_WE_N	PIN_V9	SDRAM Write Enable

DDRII

✓ Two independent DDRII SDRAM bank, maximum size up to 64M * 16bits for each bank.

DDRII SDRAM 1		
Name	PinOut	Description
DDRII_1ADDR[0]	PIN_H14	DDRII Address 0
DDRII_1ADDR[1]	PIN_E9	DDRII Address 1
DDRII_1ADDR[2]	PIN_F12	DDRII Address 2
DDRII_1ADDR[3]	PIN_C5	DDRII Address 3
DDRII_1ADDR[4]	PIN_H13	DDRII Address 4
DDRII_1ADDR[5]	PIN_E7	DDRII Address 5
DDRII_1ADDR[6]	PIN_J13	DDRII Address 6
DDRII_1ADDR[7]	PIN_C6	DDRII Address 7
DDRII_1ADDR[8]	PIN_D13	DDRII Address 8
DDRII_1ADDR[9]	PIN_C7	DDRII Address 9
DDRII_1ADDR[10]	PIN_A6	DDRII Address 10
DDRII_1ADDR[11]	PIN_E13	DDRII Address 11
DDRII_1ADDR[12]	PIN_D6	DDRII Address 12
DDRII_1BA[0]	PIN_E6	DDRII Bank Address 0
DDRII_1BA[1]	PIN_C9	DDRII Bank Address 1
DDRII_1BA[2]	PIN_C8	DDRII Bank Address 2
DDRII_1CAS_N	PIN_H11	DDRII Column Address Strobe
DDRII_1CKE	PIN_E5	DDRII Clock Enable
DDRII_1CLK_N	PIN_E15	DDRII Differential Clock P
DDRII_1CLK_P	PIN_D15	DDRII Differential Clock N
DDRII_1CS_N	PIN_J14	DDRII Chip Enable
DDRII_1DQ[0]	PIN_B10	DDRII Data 0
DDRII_1DQ[1]	PIN_F10	DDRII Data 1
DDRII_1DQ[2]	PIN_D8	DDRII Data 2
DDRII_1DQ[3]	PIN_F8	DDRII Data 3

DDRII_1DQ[4]	PIN_E8	DDRII Data 4
DDRII_1DQ[5]	PIN_D10	DDRII Data 5
DDRII_1DQ[6]	PIN_D11	DDRII Data 6
DDRII_1DQ[7]	PIN_A10	DDRII Data 7
DDRII_1DQ[8]	PIN_D12	DDRII Data 8
DDRII_1DQ[9]	PIN_G11	DDRII Data 9
DDRII_1DQ[10]	PIN_A12	DDRII Data 10
DDRII_1DQ[11]	PIN_A11	DDRII Data 11
DDRII_1DQ[12]	PIN_G10	DDRII Data 12
DDRII_1DQ[13]	PIN_G12	DDRII Data 13
DDRII_1DQ[14]	PIN_E11	DDRII Data 14
DDRII_1DQ[15]	PIN_B11	DDRII Data 15
DDRII_1DQM[0]	PIN_C10	DDRII Data Mask 0
DDRII_1DQM[1]	PIN_C12	DDRII Data Mask 1
DDRII_1DQS[0]	PIN_F9	DDRII Data Strobe 0
DDRII_1DQS[1]	PIN_F11	DDRII Data Strobe 1
DDRII_1ODT	PIN_K15	DDRII On Die Termination
DDRII_1RAS_N	PIN_C11	DDRII Column Address Strobe
DDRII_1WE_N	PIN_D5	DDRII Write Enable

DDRII SDRAM 1		
Name	PinOut	Description
DDRII_2ADDR[0]	PIN_C27	DDRII Address 0
DDRII_2ADDR[1]	PIN_H23	DDRII Address 1
DDRII_2ADDR[2]	PIN_G24	DDRII Address 2
DDRII_2ADDR[3]	PIN_J20	DDRII Address 3
DDRII_2ADDR[4]	PIN_E26	DDRII Address 4
DDRII_2ADDR[5]	PIN_H22	DDRII Address 5
DDRII_2ADDR[6]	PIN_C25	DDRII Address 6
DDRII_2ADDR[7]	PIN_G21	DDRII Address 7
DDRII_2ADDR[8]	PIN_E27	DDRII Address 8
DDRII_2ADDR[9]	PIN_G22	DDRII Address 9
DDRII_2ADDR[10]	PIN_H20	DDRII Address 10
DDRII_2ADDR[11]	PIN_C26	DDRII Address 11
DDRII_2ADDR[12]	PIN_H21	DDRII Address 12
DDRII_2BA[0]	PIN_F20	DDRII Bank Address 0
DDRII_2BA[1]	PIN_E18	DDRII Bank Address 1
DDRII_2BA[2]	PIN_D20	DDRII Bank Address 2
DDRII_2CAS_N	PIN_F24	DDRII Column Address Strobe
DDRII_2CKE	PIN_J19	DDRII Clock Enable
DDRII_2CLK_N	PIN_D16	DDRII Differential Clock P
DDRII_2CLK_P	PIN_C16	DDRII Differential Clock N
DDRII_2CS_N	PIN_D28	DDRII Chip Enable
DDRII_2DQ[0]	PIN_A21	DDRII Data 0
DDRII_2DQ[1]	PIN_E19	DDRII Data 1
DDRII_2DQ[2]	PIN_B20	DDRII Data 2
DDRII_2DQ[3]	PIN_C22	DDRII Data 3

DDRII_2DQ[4]	PIN_E20	DDRII Data 4
DDRII_2DQ[5]	PIN_C20	DDRII Data 5
DDRII_2DQ[6]	PIN_C21	DDRII Data 6
DDRII_2DQ[7]	PIN_A22	DDRII Data 7
DDRII_2DQ[8]	PIN_A23	DDRII Data 8
DDRII_2DQ[9]	PIN_C23	DDRII Data 9
DDRII_2DQ[10]	PIN_D23	DDRII Data 10
DDRII_2DQ[11]	PIN_F23	DDRII Data 11
DDRII_2DQ[12]	PIN_D21	DDRII Data 12
DDRII_2DQ[13]	PIN_F22	DDRII Data 13
DDRII_2DQ[14]	PIN_A24	DDRII Data 14
DDRII_2DQ[15]	PIN_C24	DDRII Data 15
DDRII_2DQM[0]	PIN_B21	DDRII Data Mask 0
DDRII_2DQM[1]	PIN_B23	DDRII Data Mask 1
DDRII_2DQS[0]	PIN_D19	DDRII Data Strobe 0
DDRII_2DQS[1]	PIN_D22	DDRII Data Strobe 1
DDRII_2ODT	PIN_E25	DDRII On Die Termination
DDRII_2RAS_N	PIN_J23	DDRII Column Address Strobe
DDRII_2WE_N	PIN_D18	DDRII Write Enable

JP10, JP11 and JP12

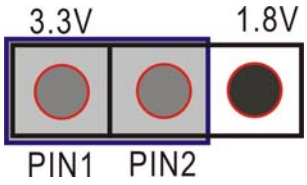
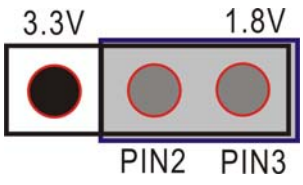
✓ Please refer to **TREX-S2** spec for the pin assignment of connector **J11 – J12**.

Connector Name	TREX-S1 Connector
JP10	**J10**
JP11	**J11**
JP12	**J12**

Jumper Setting

JP16 - VCCIO (Bank 7 & 8) Selection

✓ JP16 is used to set the VCCIO (Bank Voltage) of JP10, JP11 and JP12.

Name	I/O Banks	VCCIO (Pin 1,2 short)	VCCIO (Pin 2,3 short)
VCCB78	7 & 8	3.3V 	1.8V 

NOTE on VREF: VREF pins of BANK 7 and BANK 8 are unconnected.

JP3 – JP1 and JP2 power Selection.

✓ JP3 is used to set the power output of the JP1 and JP2.

Name	JP1 Pin_11	JP1 Pin_29	JP2 Pin_11	JP2 Pin_29
JP3 (Pin 1,2 short)	5V	X	X	X
JP3 (Pin 1,2 open)	NC	X	X	X
JP3 (Pin 3,4 short)	X	3.3V	X	X
JP3 (Pin 3,4 open)	X	NC	X	X
JP3 (Pin 5,6 short)	X	X	5V	X
JP3 (Pin 5,6 open)	X	X	NC	X
JP3 (Pin 7,8 short)	X	X	X	3.3V
JP3 (Pin 7,8 open)	X	X	X	NC

JP9 – JP7 and JP8 power Selection.

✓ JP9 is used to set the power output of the JP7 and JP8.

Name	JP7 Pin_11	JP7 Pin_29	JP8 Pin_11	JP8 Pin_29
JP9 (Pin 1,2 short)	5V	X	X	X
JP9 (Pin 1,2 open)	NC	X	X	X
JP9 (Pin 3,4 short)	X	3.3V	X	X
JP9 (Pin 3,4 open)	X	NC	X	X
JP9 (Pin 5,6 short)	X	X	5V	X
JP9 (Pin 5,6 open)	X	X	NC	X
JP9 (Pin 7,8 short)	X	X	X	3.3V
JP9 (Pin 7,8 open)	X	X	X	NC

MSEL (M3 M2 M1 M0)

✓ JP17 is to set the configuration scheme of the FPGA. The follow table is copied from Altera Stratix II handbook. Users can refer to the original document for detailed information. Note that **M3 – M0** represents **MSEL3 – MSEL0**, respectively.

To avoid any problems with detecting an incorrect configuration scheme, hard-wire the MSEL[] pins to V_{CCPD} and GND, without any pull-up or pull-down resistors. Do not drive the MSEL[] pins by a microprocessor or another device.

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0
Fast passive parallel (FPP)	0	0	0	0
Passive parallel asynchronous (PPA)	0	0	0	1
Passive serial (PS)	0	0	1	0
Remote system upgrade FPP *(1)*	0	1	0	0
Remote system upgrade PPA *(1)*	0	1	0	1
Remote system upgrade PS *(1)*	0	1	1	0
Fast AS (40 MHz) *(2)*	1	0	0	0
Remote system upgrade fast AS (40 MHz) *(2)*	1	0	0	1
FPP with decompression and/or design security feature enabled *(3)*	1	0	1	1
Remote system upgrade FPP with decompression and/or design security feature enabled *(1)*, *(3)*	1	1	0	0
AS (20 MHz) *(2)*	1	1	0	1
Remote system upgrade AS (20 MHz) *(2)*	1	1	1	0
JTAG-based configuration *(5)*	*(4)*	*(4)*	*(4)*	*(4)*

(1) These schemes require that you drive the RUnLU pin to specify either remote update or local update. For more information about remote system upgrades in Stratix II devices, refer to the chapter *Remote System Upgrades With Stratix II & Stratix II GX Devices* in Volume 2 of the *Stratix II Device Handbook* or the *Stratis II GX Device Handbook*.
(2) Only the EPCS16 and EPCS64 devices support up to a 40 MHz DCLK. Other EPCS devices support up to a 20 MHz DCLK. Refer to the *Serial Configuration Devices Data Sheet* for more information.
(3) These modes are only supported when using a MAX II device or a microprocessor with flash memory for configuration. In these modes, the host system must output a DCLK that is 4× the data rate.
(4) Do not leave the MSEL pins floating. Connect them to V_{CCPD} or ground. These pins support the non-JTAG configuration scheme used in production. If only JTAG configuration is used, you should connect the MSEL pins to ground.
(5) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

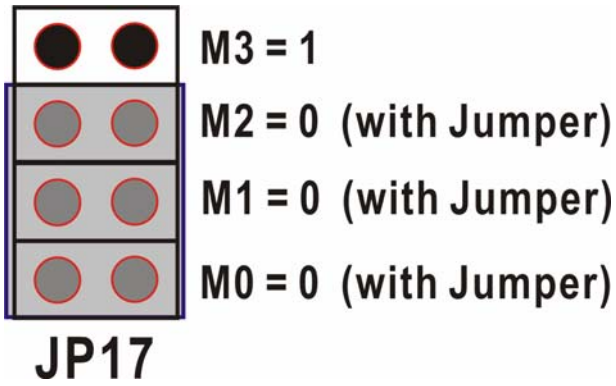


Figure 2.3. JP17 Jumper setup for **Fast AS Mode**

M0, M1 and M2=0 when jumper is connected.

M3=1 when jumper is unconnected.

Chapter 3

Electrical and Mechanical Specifications

This chapter describes the important Electrical and Mechanical specifications of TREX-S2-TMB. including how to plug or unplug the TREX-S2 from its associated main boards.

Operation and Environment Condition

This section describes the electrical specifications of **TREX-S2-TMB**

- ✓ Power Consumption: TREX-S2 module power consumption + SRAM, SDRAM and DDRII SDRAM power consumption. Please refer to the TREX-S2 user manual chapter 3 and SRAM, SDRAM and DDRII SDRAM data book.
- ✓ Power Supplier Mechanism
  - ■ DC_9V: Provide form external adapter. The maximum value for this current is 2.6A. (1.3A for EP2S60, 2.6A for EP2S180)
  - ■ VCC33: Generate form DC to DC circuit. The maximum value for this current is 10A. (3A for EP2S60, 10A for EP2S180)
  - ■ VCC18: Generate form linear regulator. The maximum value for this current is 1A.
  - ■ IO_VCC18: Generate form linear regulator. The maximum value for this current is 1A.
  - ■ DDRII_VCC18: Generate form linear regulator. The maximum value for this current is 1A.
  - ■ VCC5: Generate form linear regulator. The maximum value for this current is 1A.

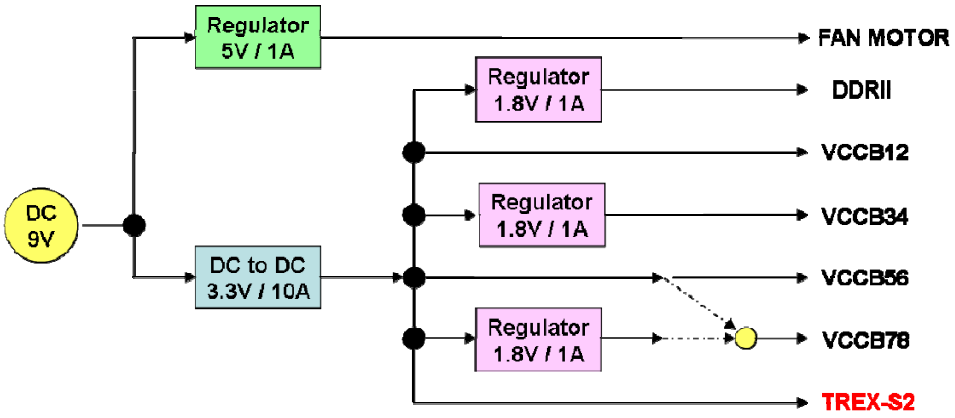


Figure 3.1 The TREX-S2-TMB power supplier scheme

TREX-S2-TMB Schematic

The CD-ROM attached includes the following files for users to create their own motherboards by modifying the schematic files of the **TREX-S2-TMB** motherboard. This is to help users to achieve their goals within the shortest time frame.

■ **CD-ROM Content**

Type and Name	CD-ROM Folder Name
TREX-S2-TMB User Manual	**TMB_user_manual**
Schematic File	**TMB_schematic**
Quartus II Porject – Default Demo	**TMB_default_demo**
Quartus II Project – Loopback	**TMB_loopback**

How to plug and unplug the TREX-S2 Module

TREX-S2 has 12 connectors for connecting itself to a motherboard. It is very difficult to unplug the module once it is installed on a motherboard. Therefore, we designed a tool to allow users to easily unplug the module from the motherboard. Please refer to Figure 3.2 for the Terasic FPGA Module Opener.

- ✓ Note that when you design your own motherboards, you need to reserve enough empty space around the connectors for the opener's stand. Please refer to **TREX-S2-TMA** spec, where we provide schematic and layout files free to our customers to shorten their design cycle.
- ✓ **Please refer to the TS2withMotherboard.pdf to get more detailed steps about how to connect and detach the TREX-S2 FPGA module with TREX-S2-TMA/TMB motherboard.**

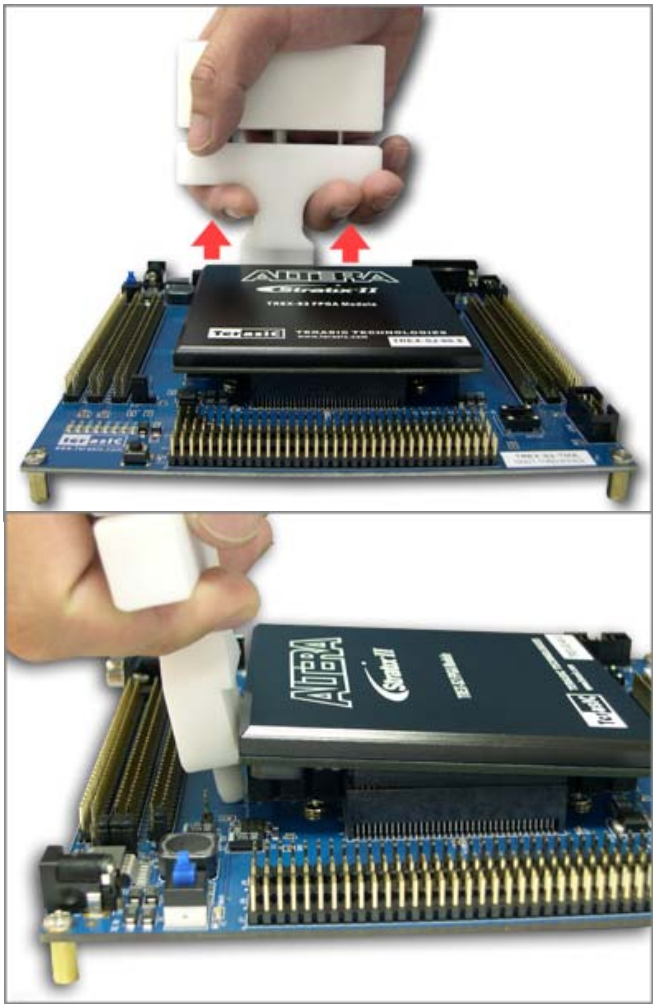


Figure 3.2 Use the Terasic FPGA Module Opener to unplug the TREX-S2 board

Chapter 4

Appendix

Part Number of Component on Board

For EP2S60 (v1.3 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
Regulator	UTC	78D05AL	U1
Regulator	NS	LM2676SX-3.3	U2
Regulator	AME	AME1117ECCTZ	U3,U4,U8
IC	MAXIM	MAX232CSET	U6
IC	Hynix	HY5PS561621AFP-33	U9,U10
IC	Hynix	HY57V561620CTP-H	U11,U12
IC	ISSI	IS61LV25616AL-10T	U13,U14
Oscillator	MEC	3SWO-AT-50.000	Y1
Oscillator	MEC	3SWO-AT-27.000	Y2
Socket	LEAMAX	21218/4PNE	Y3
Connector	SAMTEC	TFC-135-32-L-D-LC	J1~J12

For EP2S60 and EP2S180 (v1.4 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
Regulator	UTC	78D05AL	REG1
Regulator	LINEAR	LTM6400EV	REG2
Regulator	AME	AME1117ECCTZ	REG3,4 and 5
IC	ISSI	IS61LV25616AL-10T	U1,U2
IC	HYNIX	HY5PS561621AFP-33	U3,U4
IC	HYNIX	HY57V561620CTP-H	U5,U6
IC	MAXIM	MAX232CSET	U7
Socket	LEAMAX	21218/4PNE	Y1
Oscillator	MEC	3SWO-AT-50.000	Y2
Oscillator	MEC	3SWO-AT-27.000	Y3
Connector	SAMTEC	TFC-135-32-L-D-LC	J1~J12

Revision History

Date	Change Log
Apr 6, 2006 (JC)	Initial Version
Aug 15, 2006 (JC)	Update for v1.4 PCB.

Always Visit TREX-S2 Webpage for New Motherboard

We will be continuing creating various main board and labs on our DE2 webpage. Please visit TREXS2.terasic.com for more information.