

QorlQ Multicore Communications Processor Development

QorlQ T2080 Reference Design Board



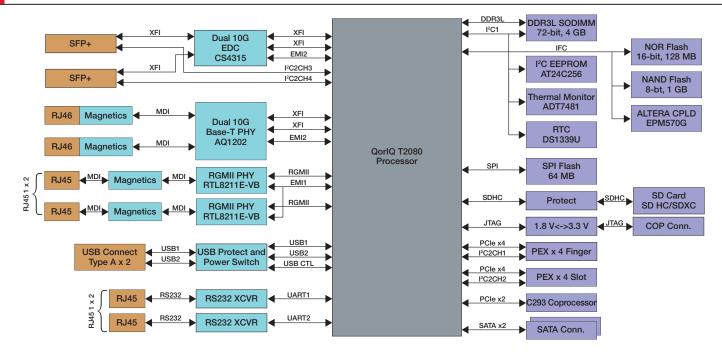
Overview

The QorlQ T2080 reference design board (T2080RDB) is a highly integrated tool featuring the QorlQ T2080 communications processor. With the high-performance T2080 processor and rich input/output (I/O) mix, the board is designed for evaluating both the

T2080 and T2081 processors in networking and Ethernet-centric applications such as high-performance control plane applications and mid-range mixed control and data plane in enterprise equipment, service provider, wireless infrastructure, aerospace and defense

and industrial computing applications. In addition, the T2080RDB contains a C293 crypto coprocessor also serving as a development platform for the C29x family of security processors.

QorlQ T2080 Reference Design Board Block Diagram







The T2080RDB can help shorten your time to market by exercising most capabilities of the device and can serve as a reference for hardware development. It can also be used as a debug tool to check behaviors on the board compared to behaviors seen on customer boards. The board can be used for software development, and performance evaluation prior to the customer's own board being ready.

The QorlQ T2080RDB comes in a 1U chassis form factor. Inside this chassis, the logic board is implemented in a PCle form factor that can be pulled out of this chassis and plugged into a host system for development of end-point applications such an intelligent NIC (iNIC) or storage adapter applications.

The T2080RDB is preloaded with the Embedded Linux® Essentials for QorlQ communications processors with Data Path Acceleration Architecture (DPAA) software development kit. This kit includes a 64-bit SMP Linux kernel, hugetlbfs for applications with a large memory footprint, user space DPAA for high-performance packet handling, U-boot, the GCC tool chain and virtualization support, among many other features.

The QorlQ T2080 communications processor is based on the 64-bit e6500 core, built on Power Architecture® technology, offering speeds of 1200-1800 MHz. These processors have a three-level cache hierarchy with 32 KB of instruction and data cache per core, 2 MB of low-latency backside shared L2 cache allowing efficient sharing of code and data and 512 KB CoreNet platform cache with a prefetch engine. The processor's I/O includes 16 SerDes lanes running at up to 10 GHz, multiplexed across four PCI Express® controllers, up to four 10 Gigabit Ethernet interfaces (XFI/KR, XaUI and HIGig), up to eight 1 Gigabit Ethernet interfaces (SGMII), two Serial RapidIO® 2.1 controllers and two SATA 2.0 interfaces.

The QorlQ T2080 communications processor also supports a 64-bit DDR3 and DDR3L (low power) SDRAM memory controller with ECC support running at up to 2133 MT/s data rate. It includes two high-speed USB 2.0 interfaces (including PHY), two DUARTs, an SD/MMC interface, a NOR/NAND controller, four I2C and SPI. It also includes the accelerator blocks collectively known as the DPAA that offload various tasks from the core, including routine packet handling, security algorithm calculation, compression, decompression and pattern matching. In addition, each e6500 core implements Freescale's AltiVec technology-based SIMD engine dramatically boosting the performance of media and networking algorithms.

QorlQ T2080RDB Board Features

Processor

- QorlQ T2080 communications processor
- Multiple SysClk inputs for generating various device frequencies

Memory

- 4 GB unbuffered DDR3 SDRAM SODIMM (64-bit bus), 1600 MHz data rate
- 128 MB NOR flash, 16-bit
- 1 GB SLC NAND flash
- SD connector to interface
- SATA interface

PCI Express

- One x4 PCle slot
- One x4 PCle gold-finger
- C293 crypto coprocessor as PCle end-point device

USB 2.0

• Dual USB slot, connected to USB PHY

Ethernet

- Dual 10 GB/s XFI—Qurtina CS4315
- Dual 10 GB/s Base-T PHY-AQ1202
- Two Independent RGMII PHYs-RTL8211

UART

• Two UART ports at up to 115200 bps

Other

- JTAG/COP for debug
- Real-time clock





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