



N-Channel 12 V and 20 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel 1	12	0.029 at V _{GS} = 4.5 V	4.5 ^a	5.6 nC
		0.034 at V _{GS} = 2.5 V	4.5 ^a	
		0.044 at V _{GS} = 1.8 V	4.5 ^a	
		0.065 at V _{GS} = 1.5 V	4.5 ^a	
Channel 2	20	0.225 at V _{GS} = - 4.5 V	1.5 ^a	1.1 nC
		0.270 at V _{GS} = - 2.5 V	1.5 ^a	
		0.345 at V _{GS} = - 1.8 V	1.5 ^a	
		0.960 at V _{GS} = - 1.5 V	0.5 ^a	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- Typical ESD Performance for Channel 2: 2800 V
- Compliant to RoHS Directive 2002/95/EC

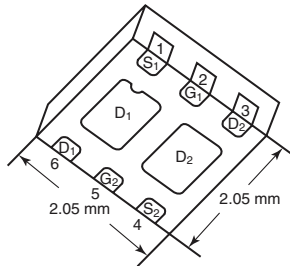


RoHS
COMPLIANT
HALOGEN
FREE

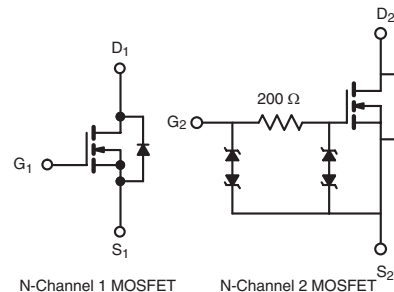
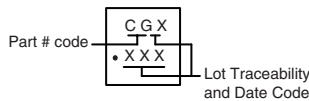
APPLICATIONS

- N-Channel Level Shift Load Switch for Portable Devices
 - for 0 V to 8 V Power Lines

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA778DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel 1 MOSFET

N-Channel 2 MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Channel 1	Channel 2	Unit	
Drain-Source Voltage	V _{DS}	12	20	V	
Gate-Source Voltage	V _{GS}	± 8	± 6		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	4.5 ^a	1.5 ^a	A
		T _C = 70 °C	4.5 ^a	1.5 ^a	
		T _A = 25 °C	4.5 ^{a, b, c}	1.5 ^{b, c}	
		T _A = 70 °C	4.5 ^{a, b, c}	1.5 ^{b, c}	
Pulsed Drain Current	I _{DM}	20	4		
Source Drain Current Diode Current	I _S	T _C = 25 °C	4.5 ^a	1.5 ^a	
		T _A = 25 °C	1.6 ^{b, c}	1.5 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	6.5	5	W
		T _C = 70 °C	5	3.2	
		T _A = 25 °C	1.9 ^{b, c}	1.9 ^{b, c}	
		T _A = 70 °C	1.2 ^{b, c}	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel 1		Channel 2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	12.5	16	20	25	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions for channel 1 and channel 2 is 110 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	12			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	20				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		12		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		21			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 2.5			
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		- 2.3			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	0.4		1	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	0.4		1		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	Ch-1			± 100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 6\text{ V}$	Ch-2			1	mA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			10		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	Ch-1	15			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	Ch-2	4				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-1		0.024	0.029	Ω	
		$V_{GS} = 4.5\text{ V}, I_D = 1.6\text{ A}$	Ch-2		0.183	0.225		
		$V_{GS} = 2.5\text{ V}, I_D = 4.6\text{ A}$	Ch-1		0.028	0.034		
		$V_{GS} = 2.5\text{ V}, I_D = 1.5\text{ A}$	Ch-2		0.220	0.270		
		$V_{GS} = 1.8\text{ V}, I_D = 4.1\text{ A}$	Ch-1		0.032	0.044		
		$V_{GS} = 1.8\text{ V}, I_D = 1.3\text{ A}$	Ch-2		0.275	0.345		
		$V_{GS} = 1.5\text{ V}, I_D = 2\text{ A}$	Ch-1		0.042	0.065		
		$V_{GS} = 1.5\text{ V}, I_D = 0.3\text{ A}$	Ch-2		0.320	0.960		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 6\text{ V}, I_D = 5\text{ A}$	Ch-1		21		S	
		$V_{DS} = 10\text{ V}, I_D = 1.6\text{ A}$	Ch-2		3.5			
Dynamic^a								
Input Capacitance	C_{iss}	Channel 1 $V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		500		pF	
Output Capacitance	C_{oss}		Ch-1		160			
Reverse Transfer Capacitance	C_{rss}		Ch-1		100			
Total Gate Charge	Q_g	$V_{DS} = 6\text{ V}, V_{GS} = 8\text{ V}, I_D = 6.5\text{ A}$	Ch-1		9.7	15	nC	
		$V_{DS} = 10\text{ V}, V_{GS} = 5\text{ V}, I_D = 1.7\text{ A}$	Ch-2		1.3	2.2		
		Channel 1 $V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$	Ch-1		5.6	8.5		
			Ch-2		1.1	1.7		
Gate-Source Charge	Q_{gs}	Channel 2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1.7\text{ A}$	Ch-1		0.72			
Gate-Drain Charge	Q_{gd}		Ch-2		0.2			
Gate Resistance	R_g	$f = 1\text{ MHz}$	Ch-1	0.7	3.5	7		Ω
			Ch-2	40	200	400		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	Channel 1 $V_{DD} = 6\text{ V}$, $R_L = 1.2\ \Omega$ $I_D \cong 5.2\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		10	15	ns
			Ch-2		20	30	
Rise Time	t_r	Channel 2 $V_{DD} = 10\text{ V}$, $R_L = 7.7\ \Omega$ $I_D \cong 1.3\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		10	15	
			Ch-2		12	20	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1		22	30	
			Ch-2		70	105	
Fall Time	t_f		Ch-1		10	15	
			Ch-2		20	30	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			4.5	A
			Ch-2			1.5	
Pulse Diode Forward Current ^a	I_{SM}		Ch-1			20	A
			Ch-2			4	
Body Diode Voltage	V_{SD}	$I_S = 5.2\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-1		0.85	1.2	V
		$I_S = 1.3\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-2		0.9	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel 1 $I_F = 5.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1		20	40	ns
			Ch-2		50	75	
Body Diode Reverse Recovery Charge	Q_{rr}	Channel 2 $I_F = 1.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1		5	10	nC
			Ch-2		30	45	
Reverse Recovery Fall Time	t_a		Ch-1		8		ns
			Ch-2		115		
Reverse Recovery Rise Time	t_b		Ch-1		12		
			Ch-2		35		

Notes:

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

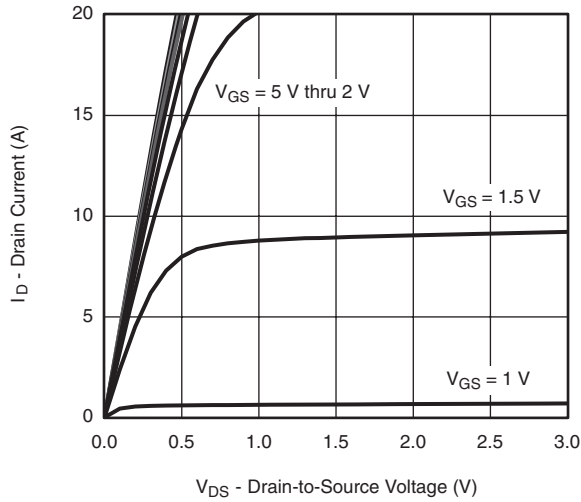
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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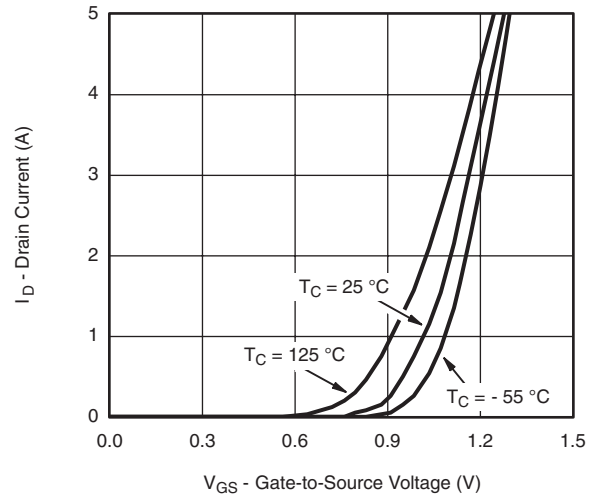
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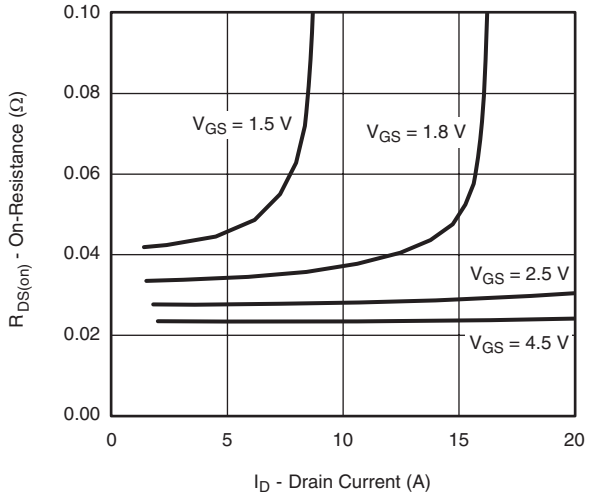
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



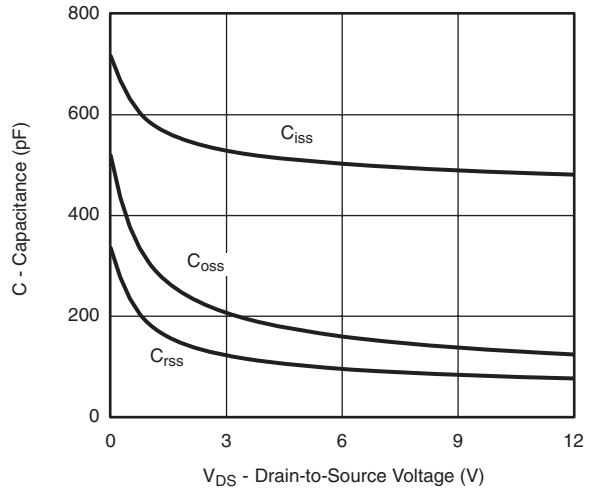
Output Characteristics



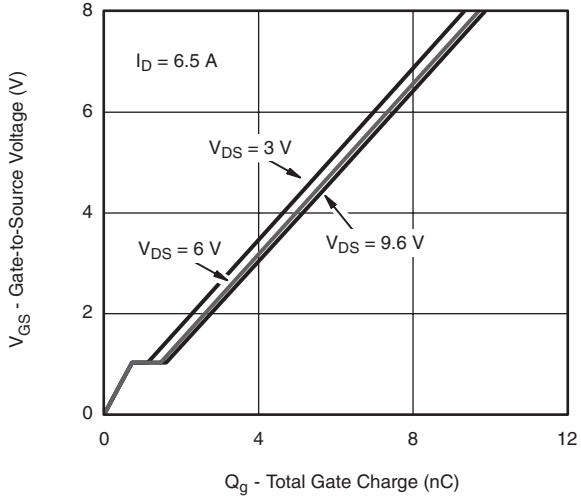
Transfer Characteristics



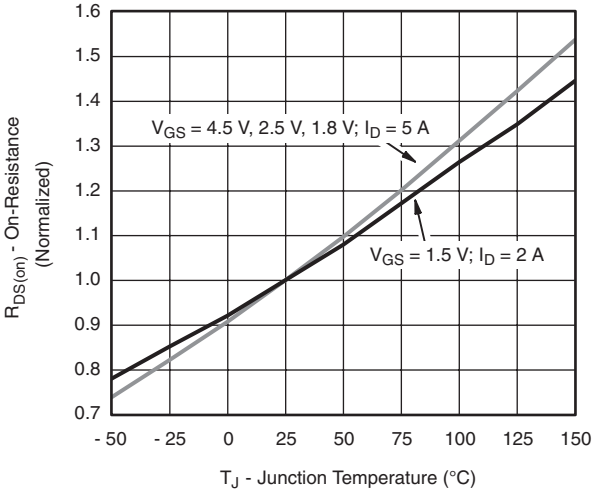
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



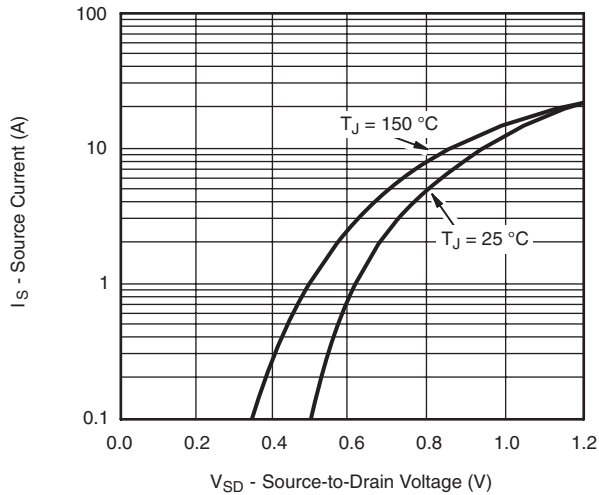
Gate Charge



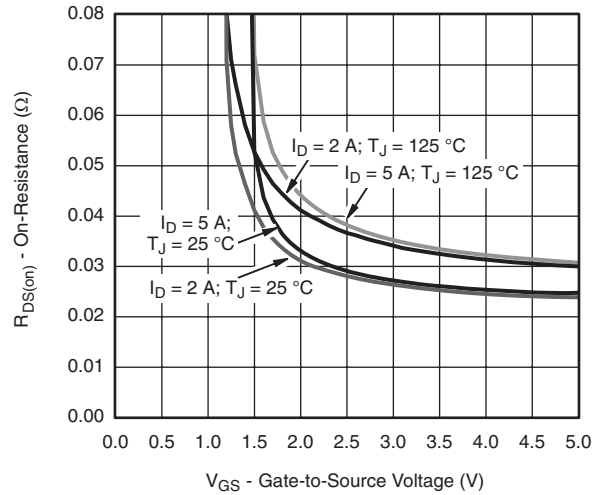
On-Resistance vs. Junction Temperature



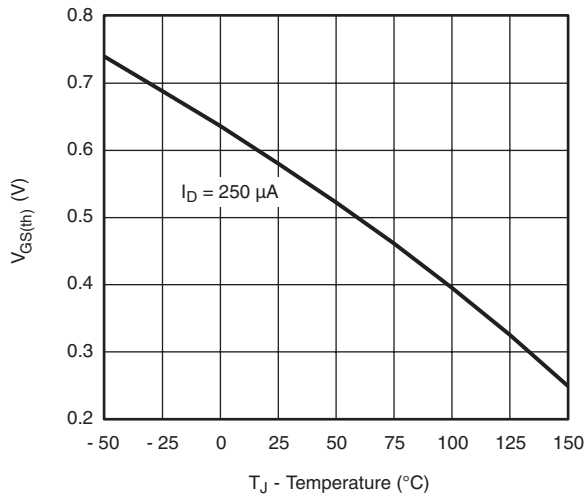
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



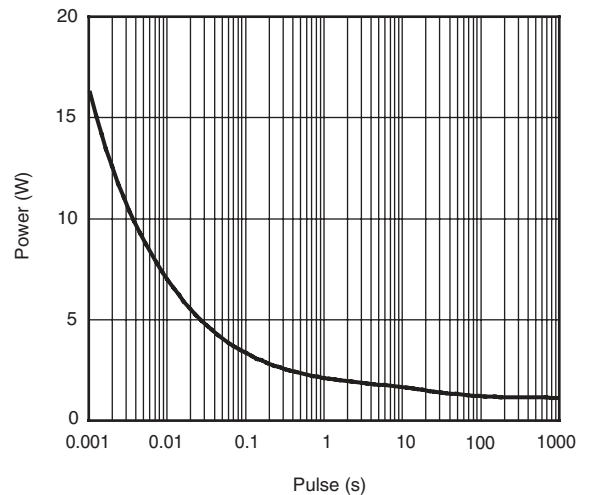
Source-Drain Diode Forward Voltage



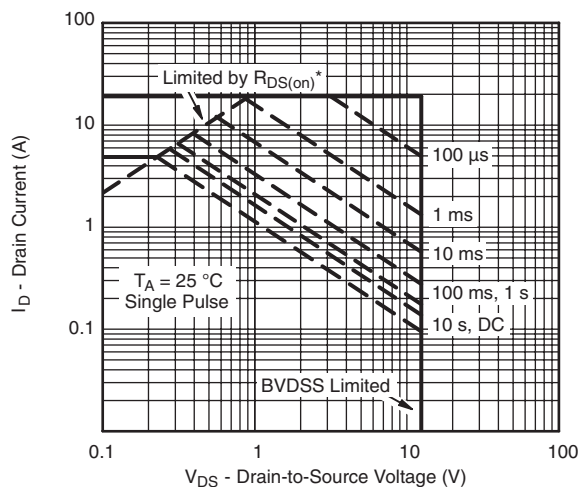
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

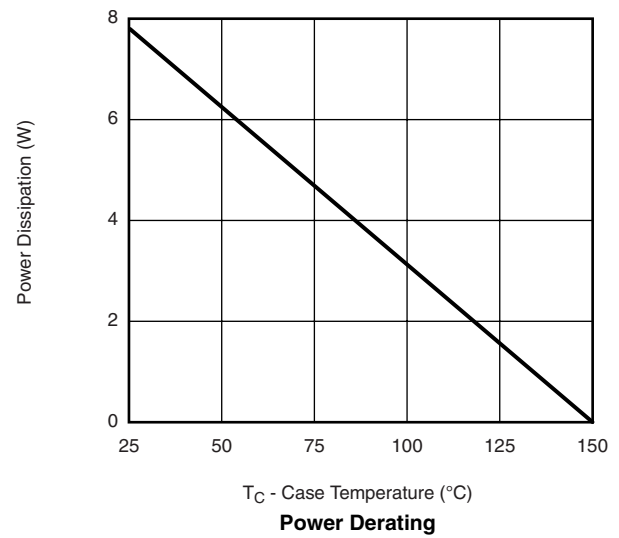
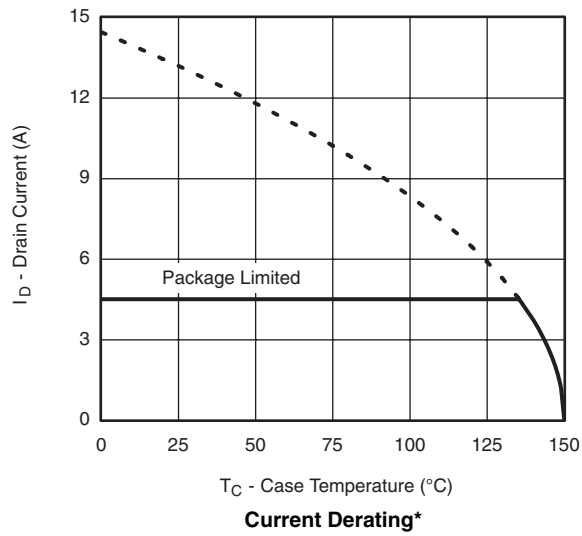


Single Pulse Power (Junction-to-Ambient)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

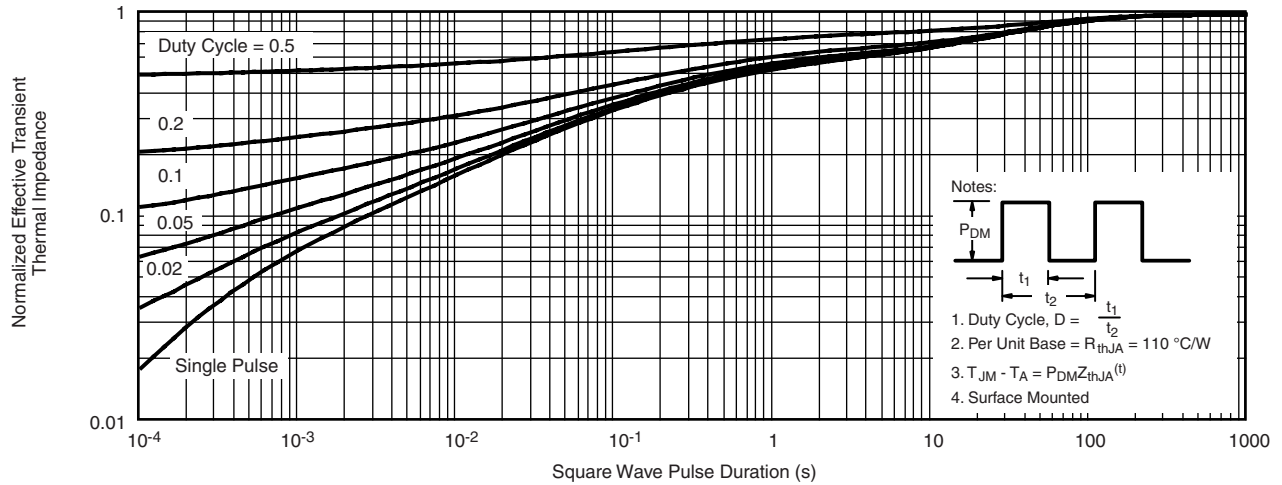
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



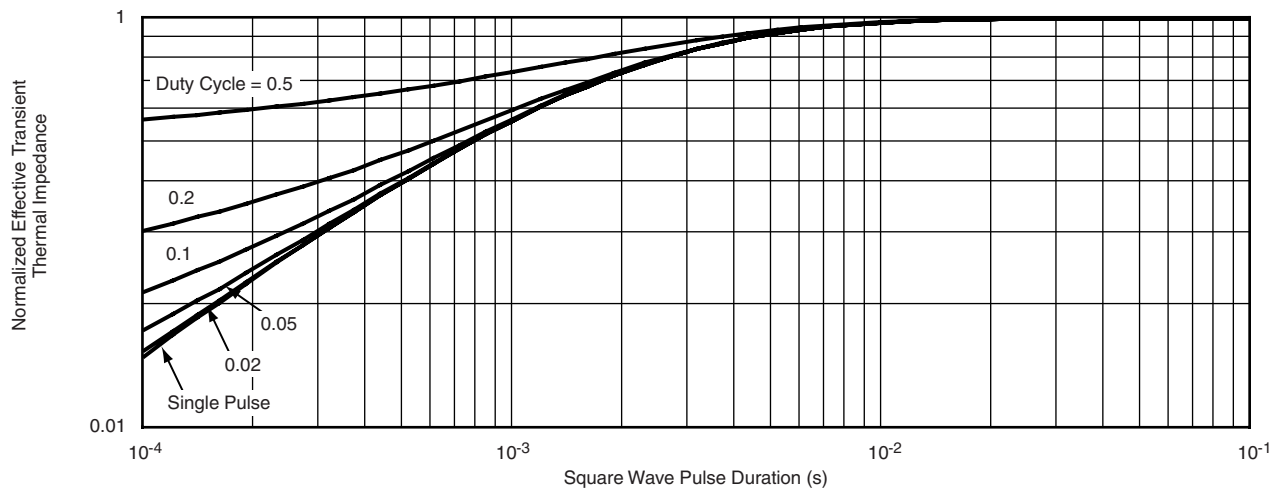
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



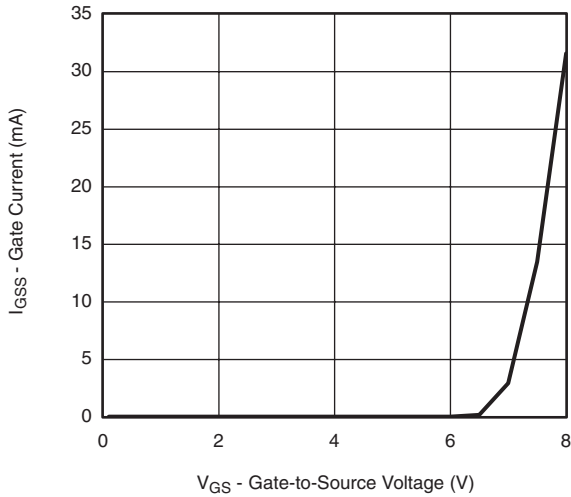
Normalized Thermal Transient Impedance, Junction-to-Ambient



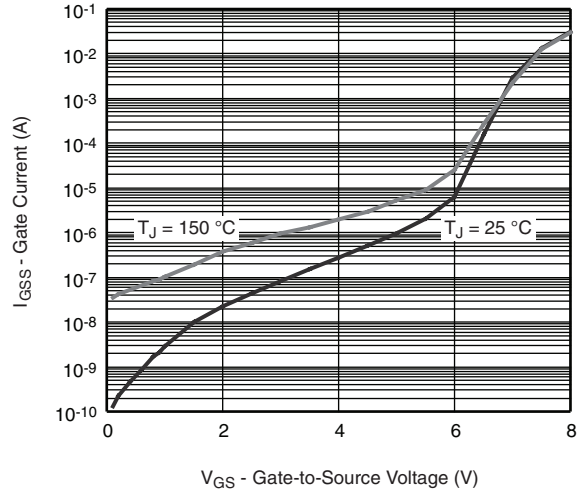
Normalized Thermal Transient Impedance, Junction-to-Case



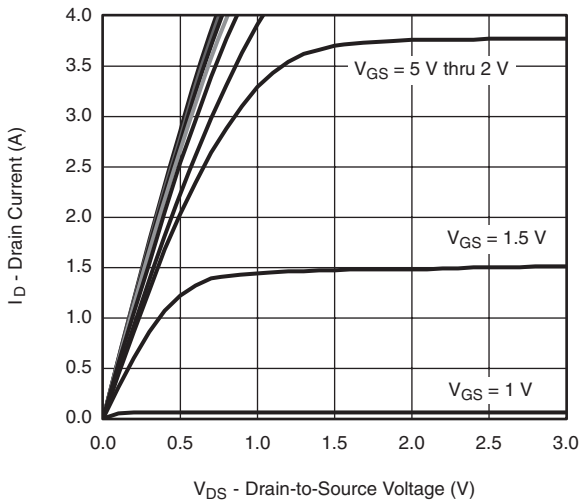
CHANNEL 2 TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



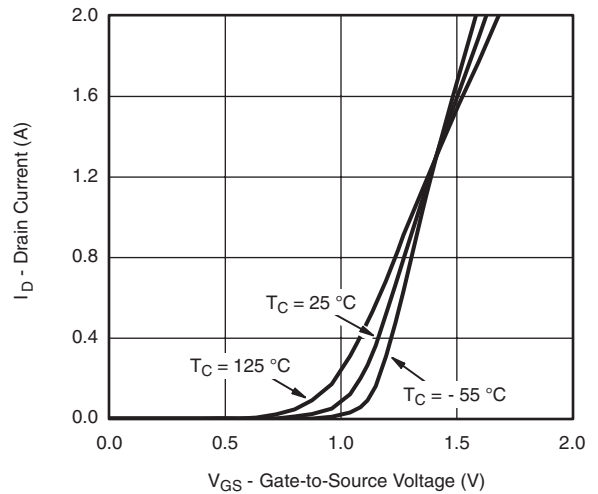
Gate Current vs. Gate-to-Source Voltage



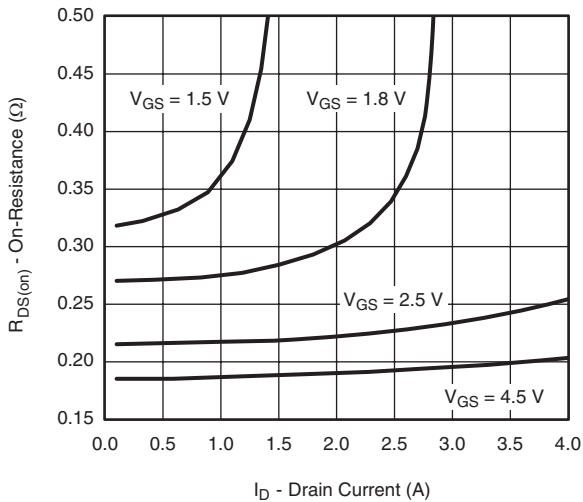
Gate Current vs. Gate-to-Source Voltage



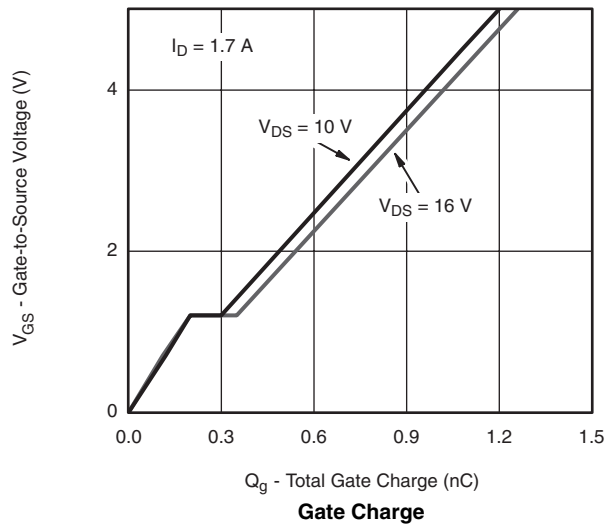
Output Characteristics



Transfer Characteristics



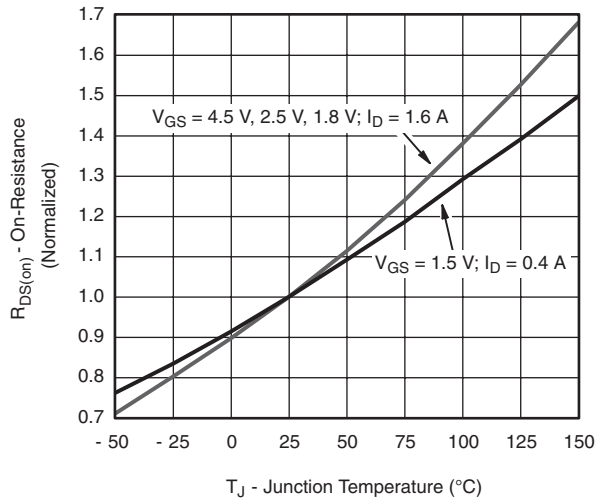
On-Resistance vs. Drain Current



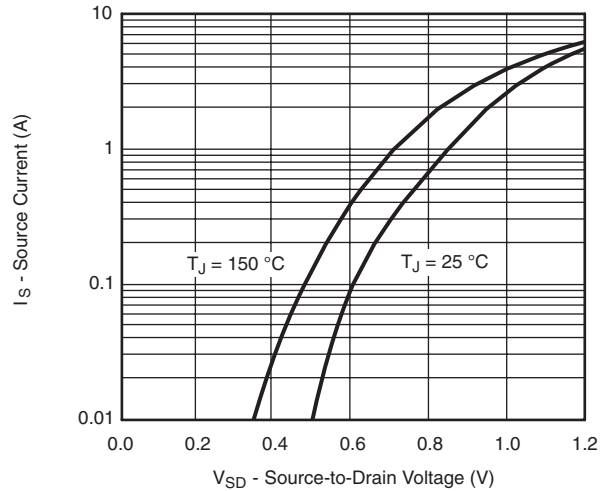
Gate Charge



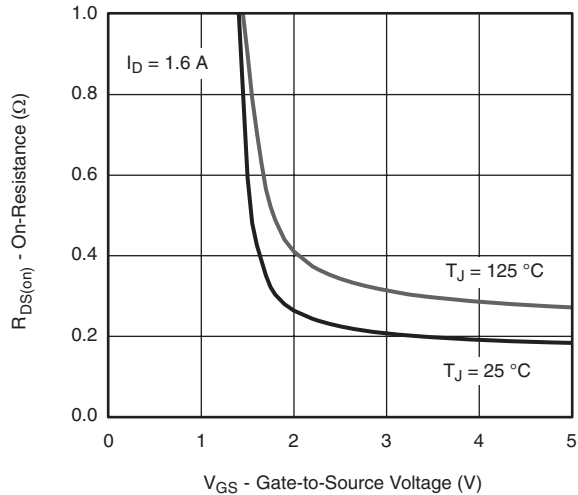
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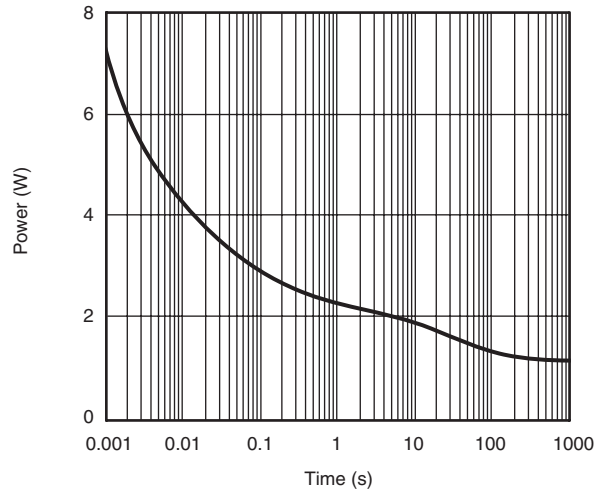
Normalized On-Resistance vs. Junction Temperature



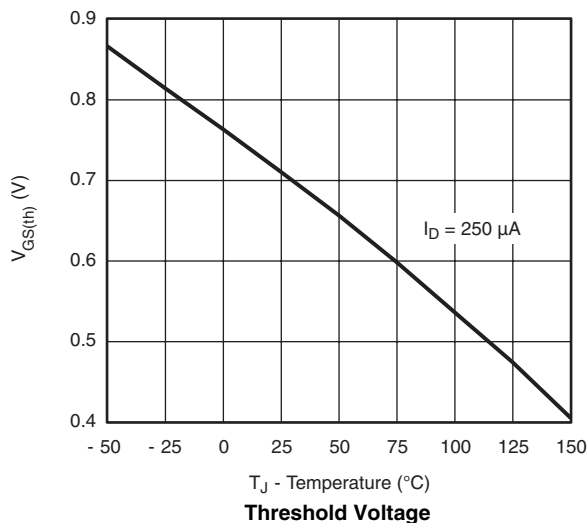
Source-Drain Diode Forward Voltage



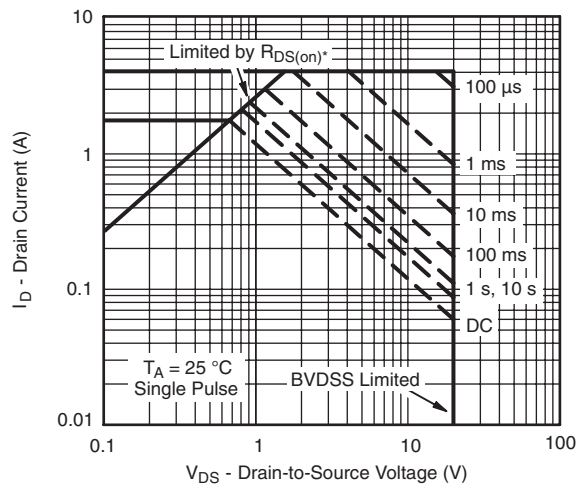
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Threshold Voltage



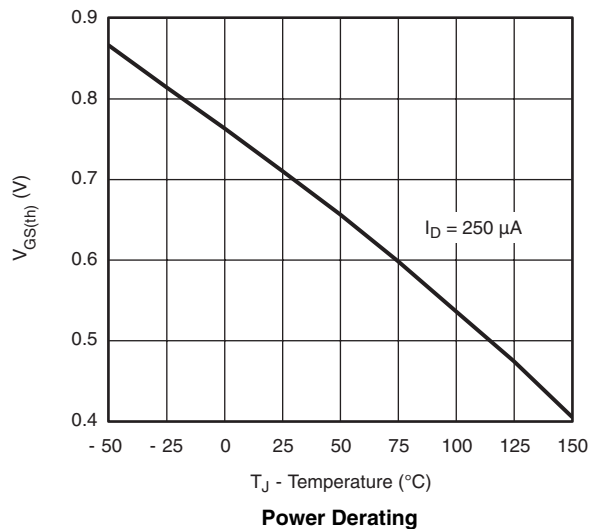
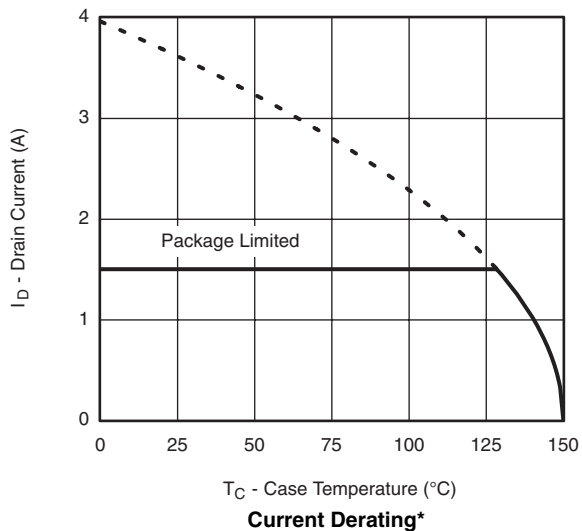
Safe Operating Area, Junction-to-Ambient
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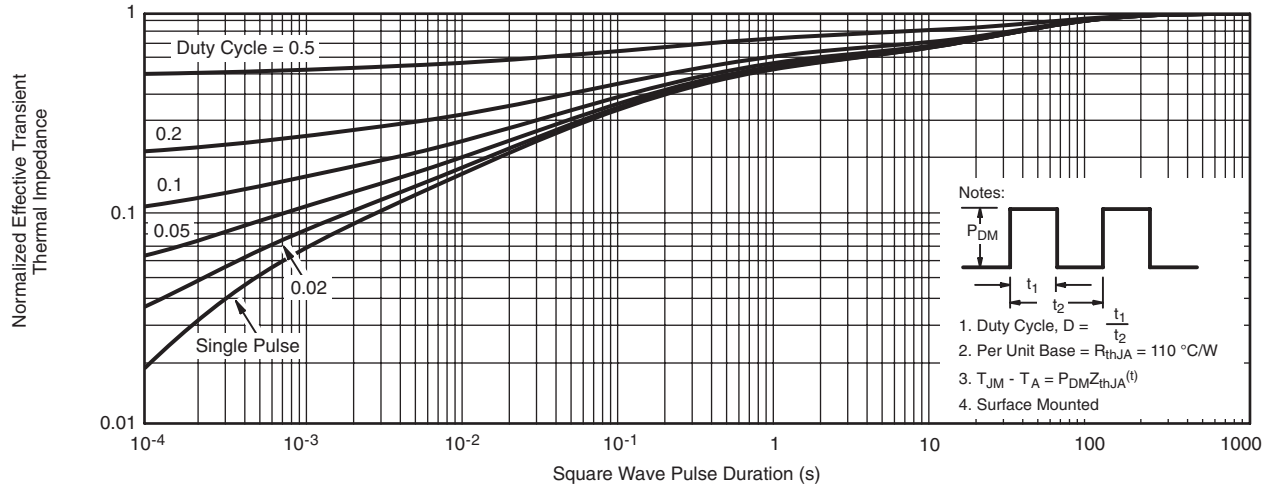
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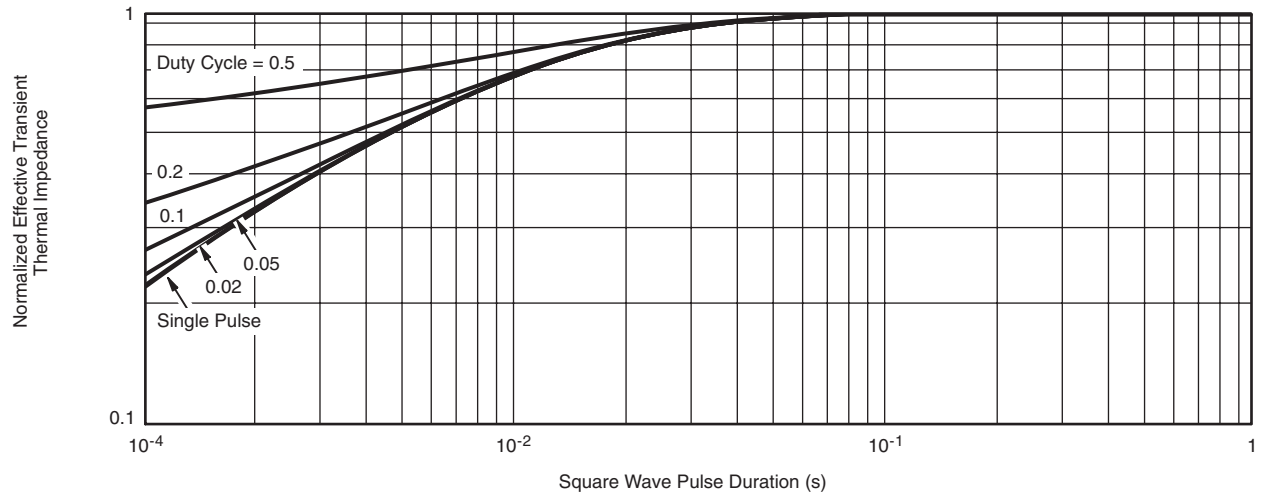
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CHANNEL 2 TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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